Tezpur University
A Central University, Government of India

Department of Electronics and Communication Engineering,
School of Engineering

REPORT

Name of Event	Hands-on Training on Advanced Digital Design with Verilog
Organized by	IEEE Student Branch and Department of Electronics and Communication Engineering, Tezpur University
Faculty Coordinators	Prof. Bhabesh Deka, Dr. Rupam Goswami
Duration	13 – 14 May 2023
Mode of Event	Online

The IEEE Student Branch, Tezpur University and the Department of Electronics and Communication Engineering, Tezpur University, hosted a two-day hands-on training on Advanced Digital Design with Verilog. The resource persons for the event were Mr. Sohail Ahmed, VLSI Verification Engineer, Cientra Techsolutions Pvt. Ltd. and Mr. Mohd. Adil, ASIC Digital Design Engineer II, Synopsys. The event started with introduction of the speakers by Prof. Santanu Sharma, Head of the Department of Electronics and Communication Engineering followed by deliberations by the depakers on introduction to VLSI: front-end and back-end profiles, and how the industry is progressing. The hands-on sessions comprised of technical explanations of fundamental combinational and sequential circuits of VLSI like multiplexer and priority encoders.

A total of 15 participants attended the event.

Faculty Coordinators Prof. Bhabesh Deka, Faculty Counselor, IEEE SB Dr. Rupam Goswami, Faculty Coordinator, IEEE SB	 Head of the Department, ECE