प्रगत संगणन विकास केंद्र
CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING
संचार एवं सूचना प्रौद्योगिकी मंत्रालय की वैज्ञानिक संस्था, भारत सरकार
A Scientific Society of the Ministry of Communications and Information Technology, Government of India

CALL for Participation Four days Technology Workshop

on

Last Date for EARLY BIRD Registration Sep. 20,2013

Hybrid Computing - Co-Processors / Accelerators- Power-aware Computing - Performance of Application Kernels

Initiatives on Measurement of Power Consumption & Performance

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Date: October 15, 2013 (Tuesday) - October 18, 2013 (Friday)
Venue: Centre for Modelling Simulation and Design (CMSD)
University of Hyderabad, Gachibowli, Hyderabad

Jointly Organized by **C-DAC, Pune University Campus & CMSD, University of Hyderabad**

http://cmsd.uohyd.ernet.in/ **REGISTRATION IS OPEN for Four Days** www.cdac.in/hypack2013/

hyPACK-2013 objective is to understand power-aware performance issues of various scientific application kernels and computational mathematics on parallel processing platforms such as computing systems with Intel Xeon-Phi Coprocessors and NVIDIA/AMD GPU accelerators as well as ARM processor based Linux multi-core processor systems. The aim is to achieve the best performance (turnaround time & throughput) and the total power consumption, a device or a system needs in order to solve a problem of given size in High Performance Computing (HPC) application kernels. The focus is to integrate different programming paradigms such as Pthreads, OpenMP, Intel TBB, Cilk Plus, Intel Xeon-Phi Offload Pragmas, MPI, NVIDIA CUDA, OpenACC,& OpenCL to extract the best achieved performance for application kernels on systems with coprocessors and accelerators. The workshop gives an opportunity to write, execute and demonstrate computational mathematics and application kernels using different programming paradigms. The workshop is aimed to cover classroom lectures in morning/forenoon session and four hours hands-on in afternoon session on every day.

Day 1 & 2 : Perf. on HPC Cluster - Intel Xeon/Phi coprocessors; ARM multi-core processor systems & Power- aware Perf. issues on HPC Cluster

- Programming on Intel Xeon-Phi Coprocessors; Xeon-Phi Coprocessor usage model : MPI vesus Offload; Compiler and Programming model; Approaches to Vectorization – Complier Directives; Prog. Paradigms – OpenMP, Intel TBB, Intel Cilk Plus, Intel MKL, MPI, OpenCL; Intel Xeon-Phi Coprocessor Architecture; Linux OS on Coprocessor; Coprocessor System software; Tuning Memory Allocation Performance – Huge Page Sizes; Profiling & Tuning- Intel Tools; PAPI; MPI
- Tuning & Performance Issues- Measurement of Power Consumption for Application Kernels - using external Power-Off-Meter; Prog. on ARM multi-core processor systems; Energy Efficiency & Performance Issues- Application Kernels; Heterogeneous Prog. - OpenCL - OpenMP 3.0 & OpenMP 4.0

Day 3 & 4: Perf. on HPC Cluster – Accelerators (NVIDIA GPUs & AMD GPUs); ARM multi-core processor systems; Hybrid Computing Platforms

- An Overview of CUDA - NVIDIA GPUs : CUDA SDK/APIs; CUDA – Optimization & Performance Issues; Efficient use of different memory types, (CUBLAS, CUFFT, CULA Tools, MAGMA, CUSPARSE, Thurst); CUDA-OpenACC APIs; Prog. - OpenCL; CUDA NVIDIA GPU Cluster; NVIDIA NVML Lib. Kepler GPU;
- An Overview of AMD Accelerated Parallel Processing (APP) Capabilities; AMD APUs - OpenCL Prog. On Multi-Core CPUs & Multi-GPUs; AMD APP Math Libraries - BLAS & FFTs; AMD APP SDK; AMD tools – Aparapi AP; AMD OpenCL tuning – performance; HPC AMD GPU Cluster: Host CPU (Pthreads, OpenMP, MPI) & OpenCL on AMD GPUs; GPU Cluster – Health Monitoring & Efficient use of GPU Cluster - MPI-OpenCL; MAGMA & Top-500 Benchmarks;
- Programming on ARM Processor multi-core systems; power-aware performance issues on ARM Multi-Coprocessor systems; Prog. on carma - NVIDIA CUDA on ARM Development Kit; An Overview of FPGA Device Systems; Energy Efficiency – Power-Off Meters & NVML Libraries - Health Monitoring - NVML Power Efficient APIs – Performance Issues; NVIDIA ARM Processor carma DevKit; Heterogeneous Prog.- Performance of Numerical Comps. kernels -OpenCL & CUDA

Application Kernels : Mixed Programming for Numerical /Non-Numerical Computations on multi-core processors with Intel Xeon-Phi coprocessors; NVIDIA /AMD GPU accelerators and ARM processor systems; Performance of Application & System Benchmarks; Image Processing Applications ; Bio-Informatics - String Search Algorithms & Sequence Analysis; Dense /Sparse Matrix Comp. on HPC GPU Cluster; Solution of Partial Diff. Eqs. (FDM &FEM); FFT Libraries; Invited Lectures on Information Sciences; Computational Physics; Computational Mathematics

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Registration Fee (in Rs.) Organization/ Institute (*)	Four Days: October 15-18 One Participant (*) (Rs.)	
	Early Bird	Regular
Private Sectors	16,000/-	18,000/-
Public Sectors/Govt. R&D Organizations	12,000/-	14,000/-
Staff from Govt. aided Universities and Colleges*	10,000/-	12,000/-
Students*	6,000/-	8,000/-

* **Limited number of grant** is available which covers travel, accommodation, and concessional registration fee for deserving candidates from govt. aided Indian universities/colleges and educational Institutes. Candidates who would like to avail this offer are requested to send soft-copy of the curriculum vitae (CV) and soft-copy of an authorization letter from the head of the Institute or dept. of the university/institute to the email-id **hypack2013@cdac.in** before **September 20, 2013**. Submitted applications will be screened and ONLY selected candidates will be intimated before **September 20, 2013** to pay the concessional registration fee. Students who are pursuing doctoral degree or in M.Tech/M.S in Parallel Computing application area of research in Govt. aided colleges will be preferred. Last date to avail this offer and **Early Bird Registration** is **September 20, 2013.**
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Accommodation: Limited guesthouse facility (as indicated in Category-1, Category-2 & Category-3) in Lakeview Guest House, University of Hyderabad (UoH) is provided for students and academic staff from Govt. aided Indian Universities/Colleges & Educational Institutes on ***first-cum-first-serve*** basis. The tariff charges are approximate. The tariff charges for Category-4 accommodation does **not** include luxury tax and participants are requested to pay the luxury tax as per tariff rates. C-DAC may provide double occupancy in UoH Guesthouses/ C-DAC booked private service apartments for participants, at participant's cost, subject to availability, upon registration before **September 20, 2013.** The ***hy*PACK-2013** registration fee does **not** include accommodation charges and will have to be borne separately by the participant. Participants are requested to pay the charges for break-fast, dinner & room services as per UoH guesthouse.

Approximate Charges per day Single/Double Occupancy in LakeView Guest House Blocks of UoH & Pvt Service Apartments				
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Single (in Rs.)	NA	NA	NA	1500/-
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Who should attend?: Graduate Students, Ph.D Scholars, faculty members, scientists, and software developers, seeking to develop software on HPC Cluster with Intel Xeon-Phi Coprocessors and GPU accelerators Knowledge of Fortran, C, C++ prog., MPI & experience on Parallel Processing platforms are mandatory pre-requisites for this tech. workshop.

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For more information Contact

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