C-DAC Four Days Technology Workshop

ON

Hybrid Computing – Coprocessors/Accelerators
Power-Aware Computing – Performance of Applications Kernels

hyPACK-2013
Mode 3 : Intel Xeon Phi Coprocessors

Lecture Topic :
Intel Xeon-Phi Coprocessor : Prog. Env

***Venue** : CMSD, UoHYD ; **Date** : October 15-18, 2013*

An Overview of Prog. Env on Intel Xeon-Phi

Lecture Outline

Following topics will be discussed

- Understanding of Intel Xeon-Phi Coprocessor Architecture
- Programming on Intel Xeon-Phi Coprocessor
- Performance Issues on Intel Xeon-Phi Coprocessor

Intel Xeon Phi - Coprocessor :

Multi-to-May-Core Processors : Background

How to run Programs faster ?

You require Super Computer

Era of Single - Multi-*to*-Many Core - Heterogeneous Computing

Sequential Computing

- Fetch/Store
- Compute

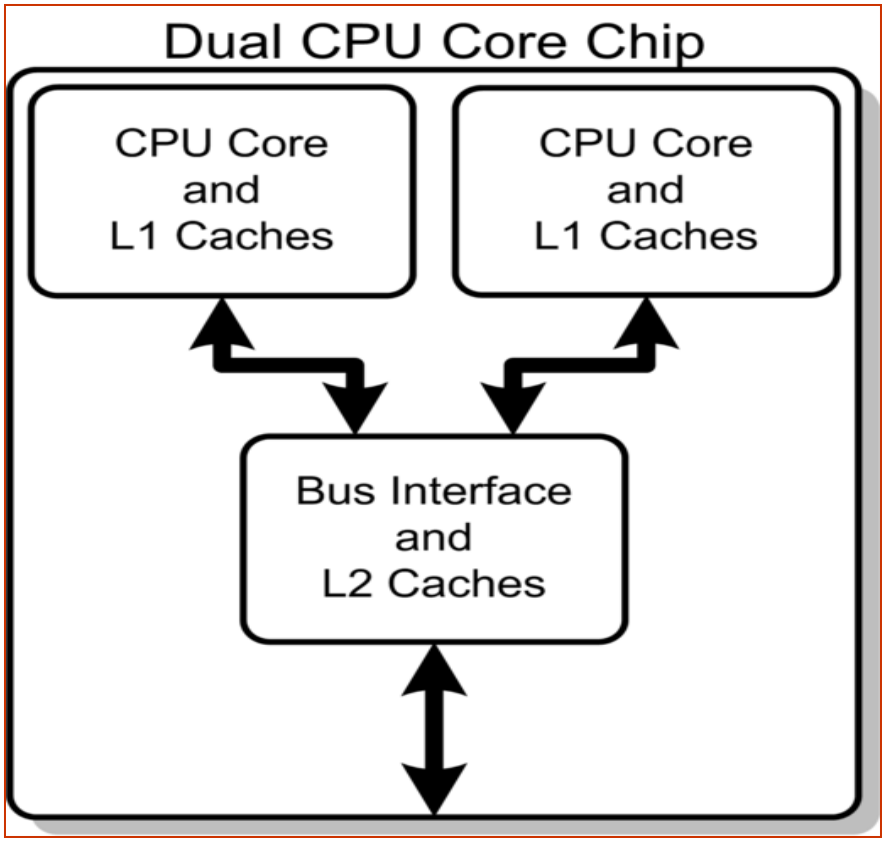
How to run Programs faster ?

- Fast Access of data
- Fast Processor
- More Memory to Manage data

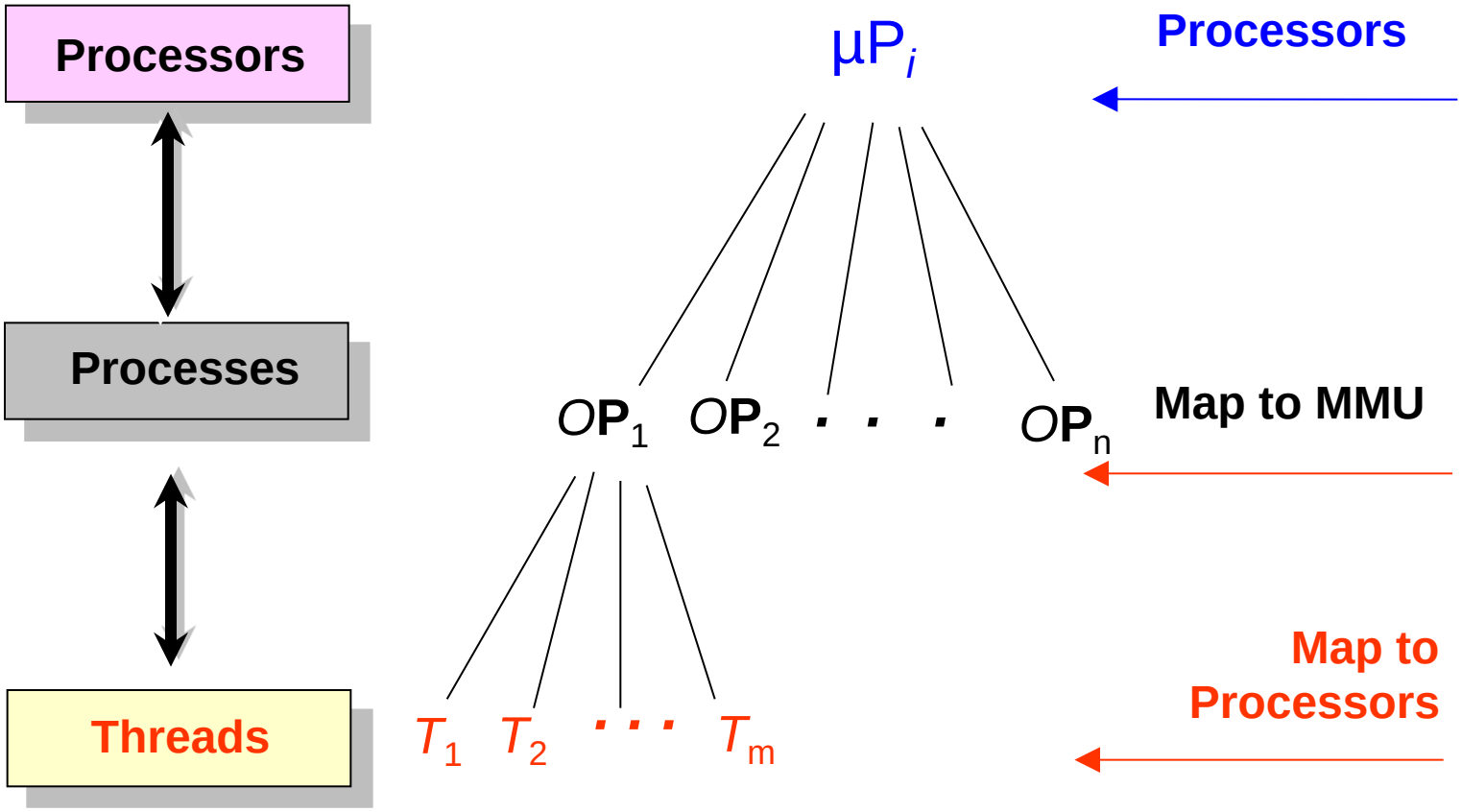
Dual Core Processor

Conceptual diagram of a dual-core CPU, with

- CPU-local Level 1 caches, and
- Shared, on-chip Level 2 caches



Relationship among Processors, Processes, &Threads

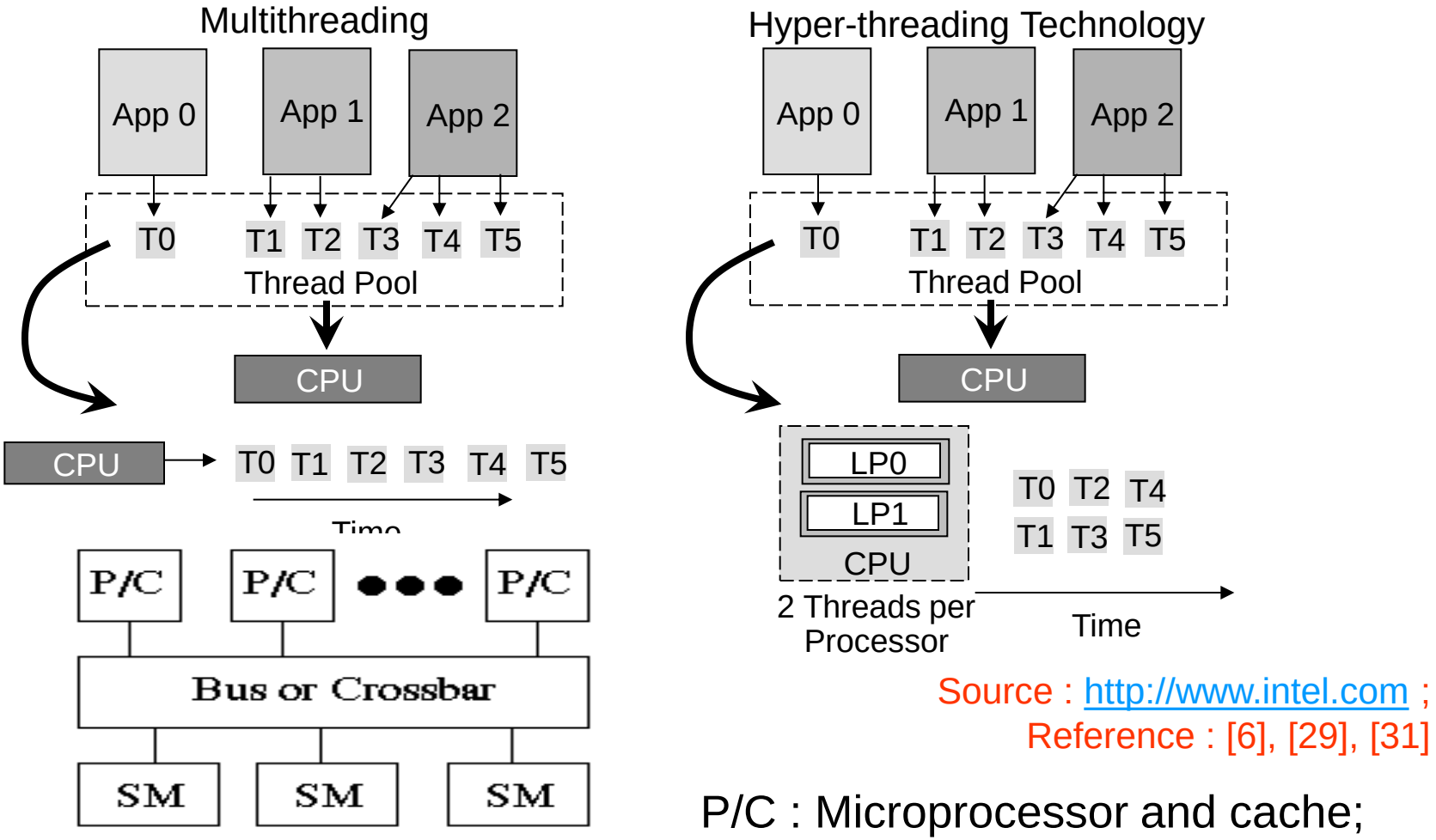


μP$_i$: Processor **OP**$_1$: Process T_1 : Thread **MMU** : Main Memory Unit

Source : Reference [4],[6], [7]

Multi-threaded Processing using Hyper-Threading Technology

- Time taken to process *n* threads on a single processor is significantly more than a single processor system with HT technology enabled.



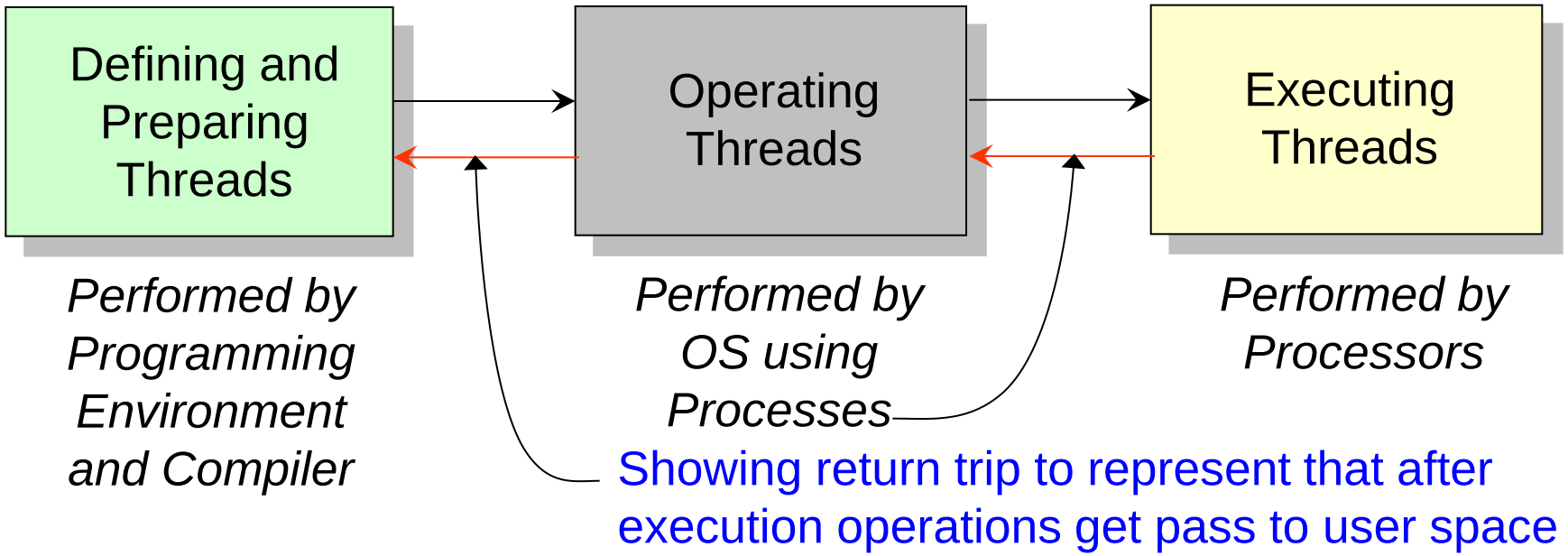
Source : http://www.intel.com ;
Reference : [6], [29], [31]

P/C : Microprocessor and cache;
SM : Shared memory

System View of Threads

Threads Above the Operating System

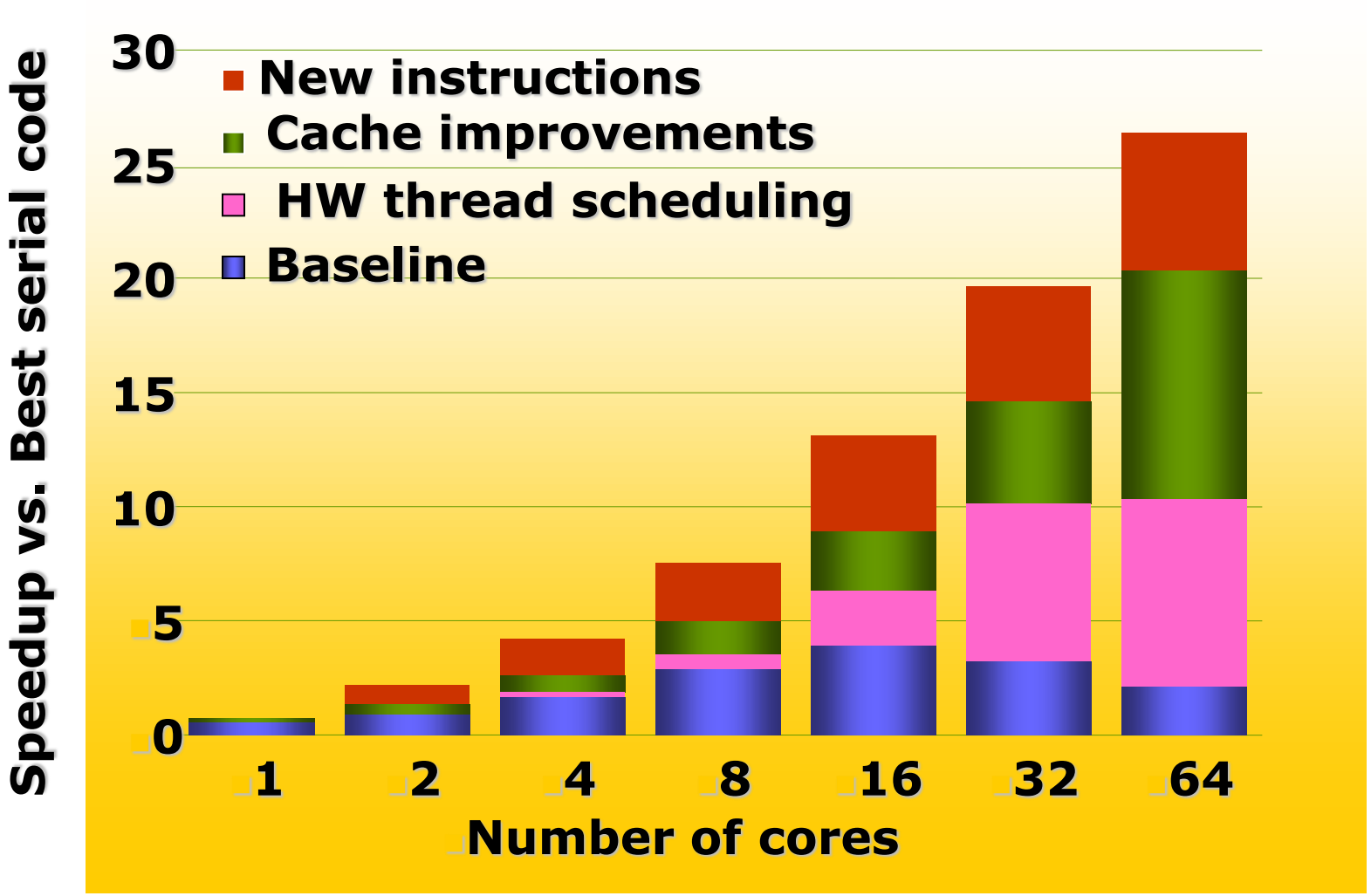
- Understand the problems - Face using the threads – Runtime Environment



Flow of Threads in an Execution Environment

Source : Reference [4],[6], [7]

Architecture-Algorithm Co-Design



Source : http://www.intel.com

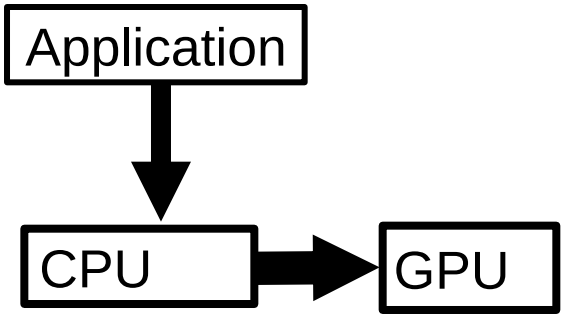
GPU Computing : Think in Parallel

- **Performance = parallel hardware**

+

scalable parallel program

- GPU Computing drives new applications
  - Reducing "Time to Discovery"
  - 100 x Speedup changes science & research methods
- New applications drive the future of GPUs
  - Drives new GPU capabilities
  - Drives hunger for more performance

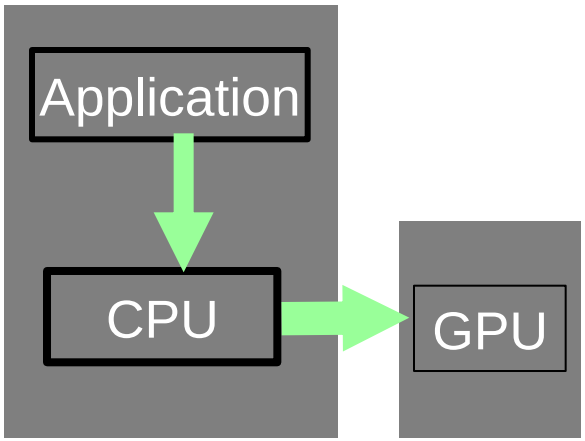


Source : NVIDIA, AMD,References

Programming paradigms-Challenges
Large scale data Computing – Current trends

Accelerators – GPU : Think in Parallel

- Speedups of 8 x to 30x are quite common for certain class of applications
- Best results when you "**Think Data Parallel**"
  - Design your algorithm for data-parallelism
  - Understand parallel algorithmic complexity and efficiency
  - Use data-parallel algorithmic primitives as building blocks

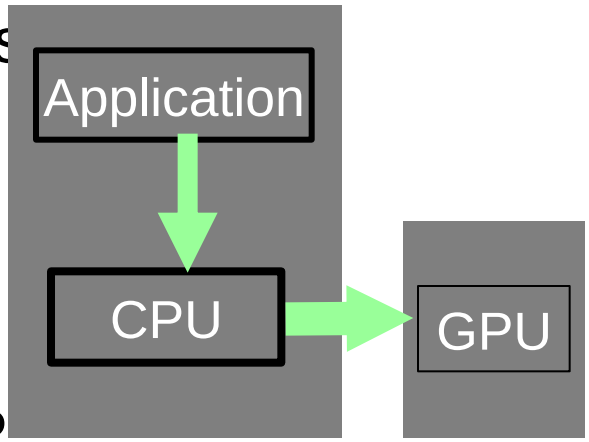


Source : NVIDIA, AMD, References

Accelerator Computing : Think in Parallel

Accelerators –GPU : Think in Parallel

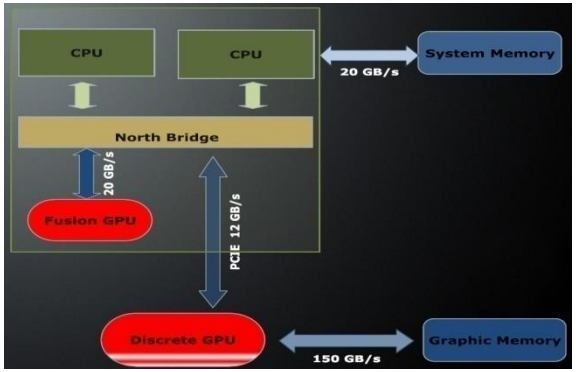
- Speedups of 8 x to 30x are quite common for certain class of applications
- The GPU is a data-parallel processor
  - Thousands of parallel threads
  - Thousands of data elements to proces
  - All data processed by the same program
  - SPMD computation model
  - Contrast with task parallelism and ILP



Source : NVIDIA, AMD, References

Systems with Accelerators

A set (one or more) of very simple execution units that can perform few operations (with respect to standard CPU) with very high efficiency. When combined with full featured CPU (CISC or RISC) can accelerate the “nominal” speed of a system.



CPU

ACC

Single thread perf.

throughput

CPU ACC.

Physical integration

CPU & ACC

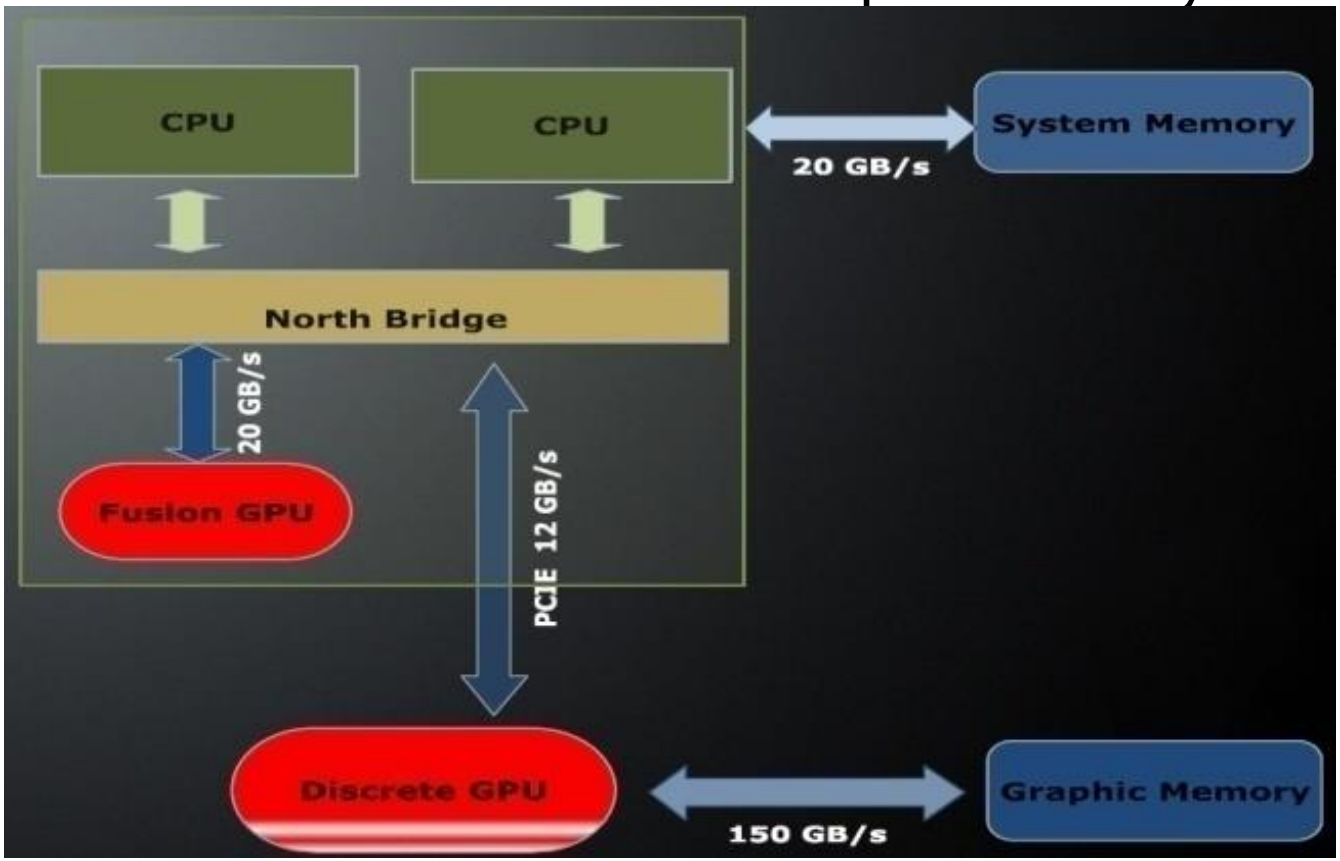
Architectural integration

CPU : Control Path & Data Path
ALU : Arithmetic and logic units
ACC: Accumulator
PC : Program counter
Micro-Instructions (Register transfer)

Source : NVIDIA, AMD, SGI, Intel, IBM Alter, Xilinux References

Systems with Accelerators

A set (one or more) of very simple execution units that can perform few operations (with respect to standard CPU) with very high efficiency. When combined with full featured CPU (CISC or RISC) can accelerate the “nominal” speed of a system.



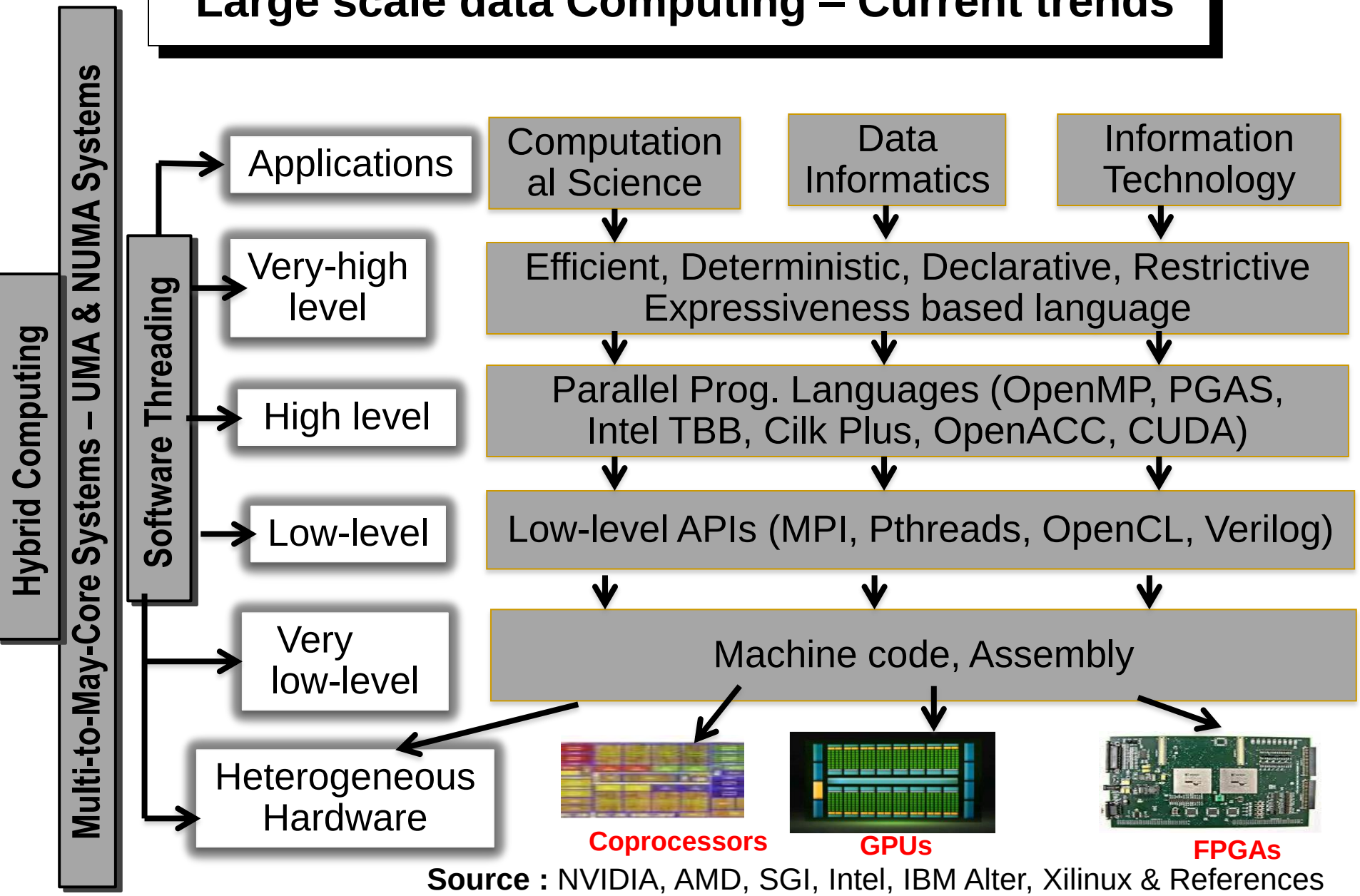
Source : NVIDIA, AMD, SGI, Intel, IBM Alter, Xilinux References

Multi-Core Systems with Accelerator Types (partial set)

- **FPGA**
  - Xilinx, Alter
- **GPU**
  - Nvidia (Kepler),
  - AMD Trinity APU
- **MIC (Intel Xeon-Phi)**
  - Intel Xeon-Phi (MIC)

Source : NVIDIA, AMD, SGI, Intel, IBM Alter, Xilinux References

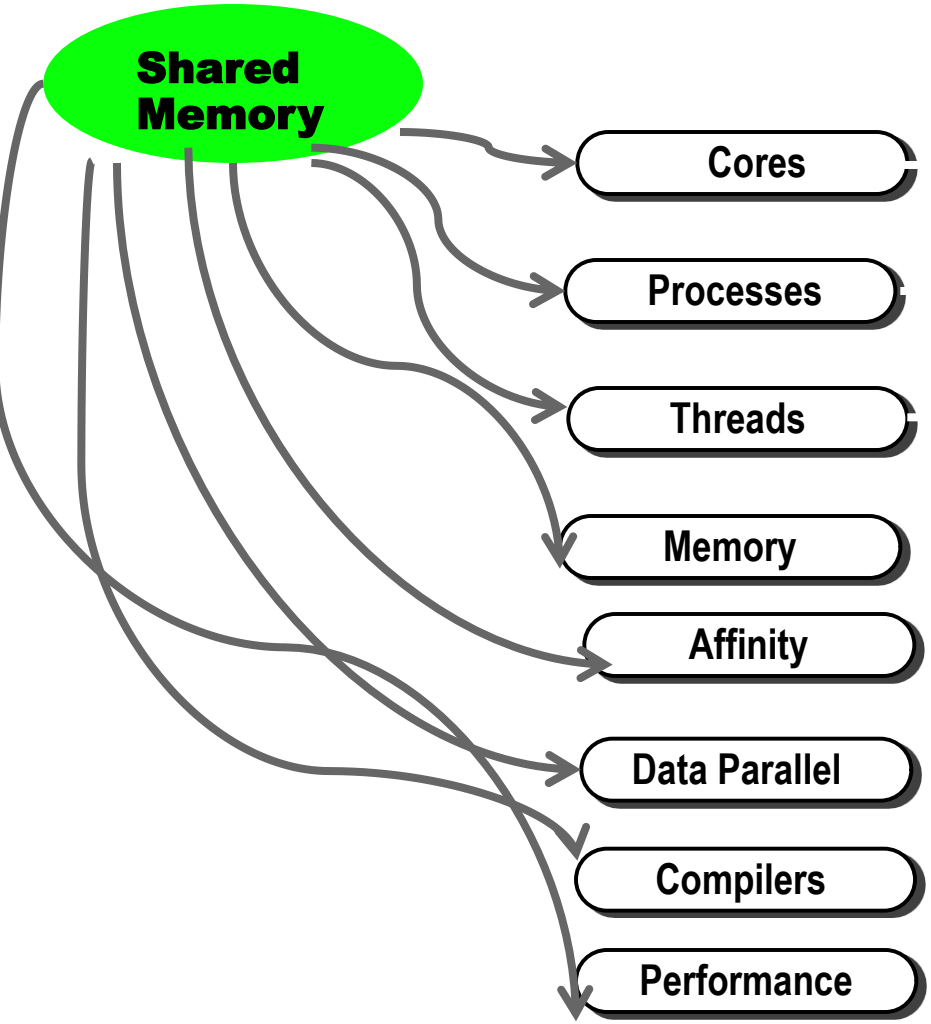
Programming paradigms-Challenges
Large scale data Computing – Current trends



Source : NVIDIA, AMD, SGI, Intel, IBM Alter, Xilinux & References

Programming paradigms-Challenges
Large scale data Computing – Current trends

Typical UMA /NUMA Computing Systems



System updates & Performance

Improvements
Quantify impacts prior to implementation

Is the machine working ?
Performance be expected

Small prototype available
What will be the performance of system ?

System available for measurement
What will be performance for App

Resources Availability
Application Scaling – Resources Avilable

.....

.....

Programming API - Multi-Core Systems with Accelerator Types (partial set)

- DO Parallel
- DO Synchronize
- Get Maximum of all values
- Give to Compiler

- DO TRANSFER from Host to Device
- Perform C omp. On Device

- Use as Linux OS
- DO TRANSFER from Host to Device

Parallel Prog. Languages (OpenMP, PGAS, Intel TBB, Cilk Plus, OpenACC, CUDA)

Programming with High Level APIs

Host : Multi-Core Systems OR ARM Multi-core Systems

CPU- Multi-Core Sys With

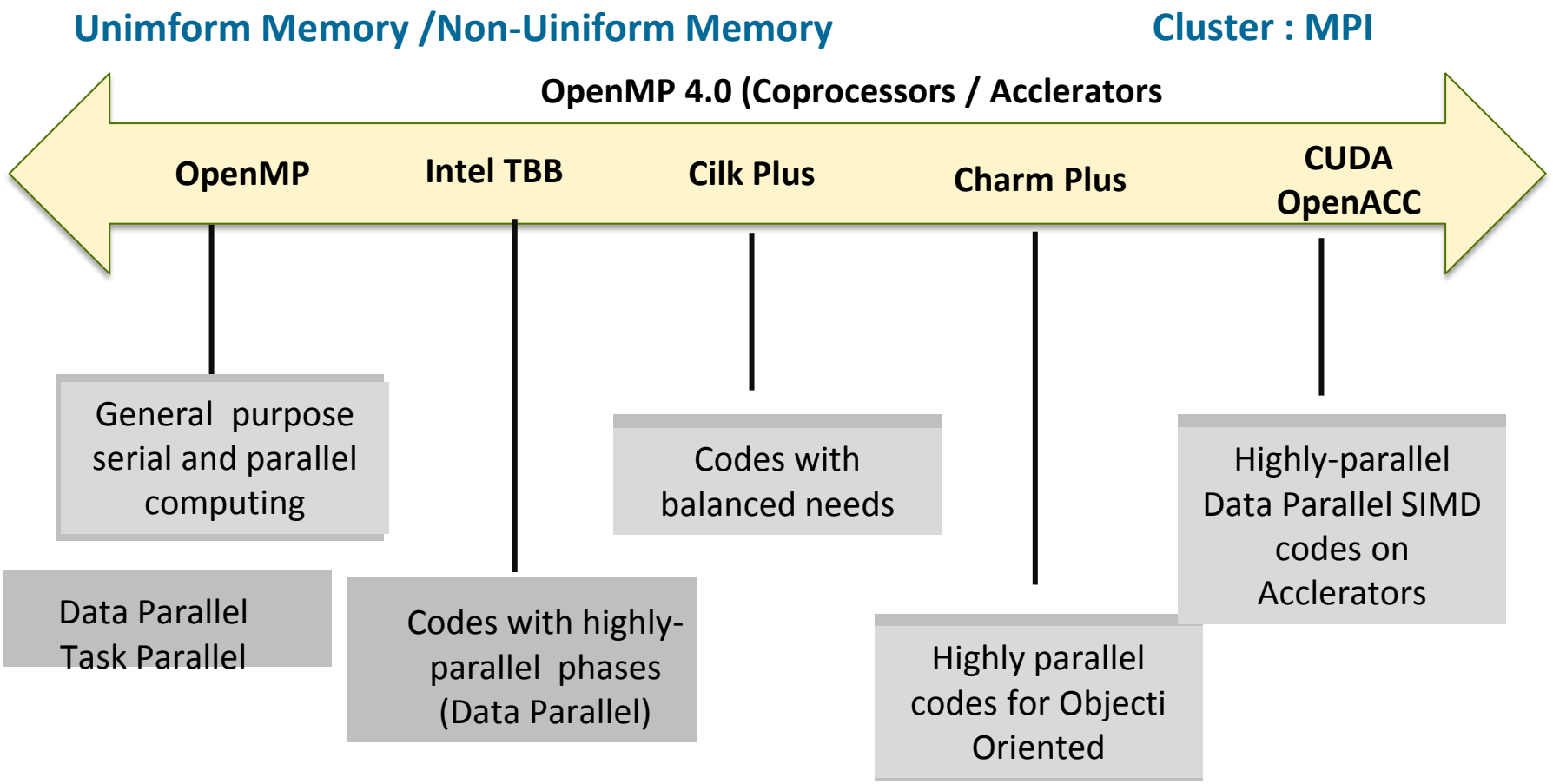
FPGA (Xilinx, Alter)

GPU - Nvidia (Kepler), AMD Trinity APU

MIC (Intel Xeon-Phi)

Source : NVIDIA, AMD, SGI, Intel, IBM Alter, Xilinux References

Prog. On Hybrid Computing Platforms

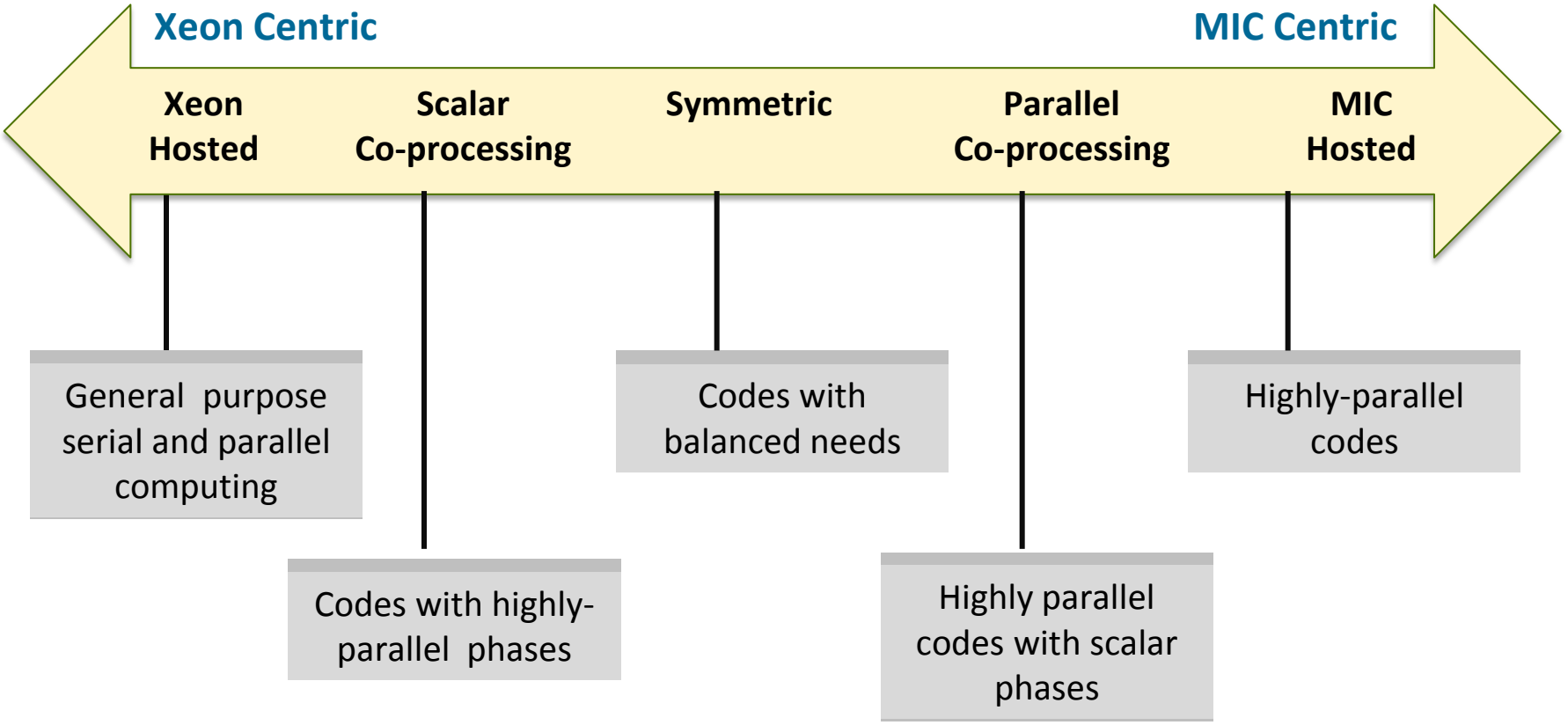


Source : References & NVIDIA, ntel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi - Coprocessor :

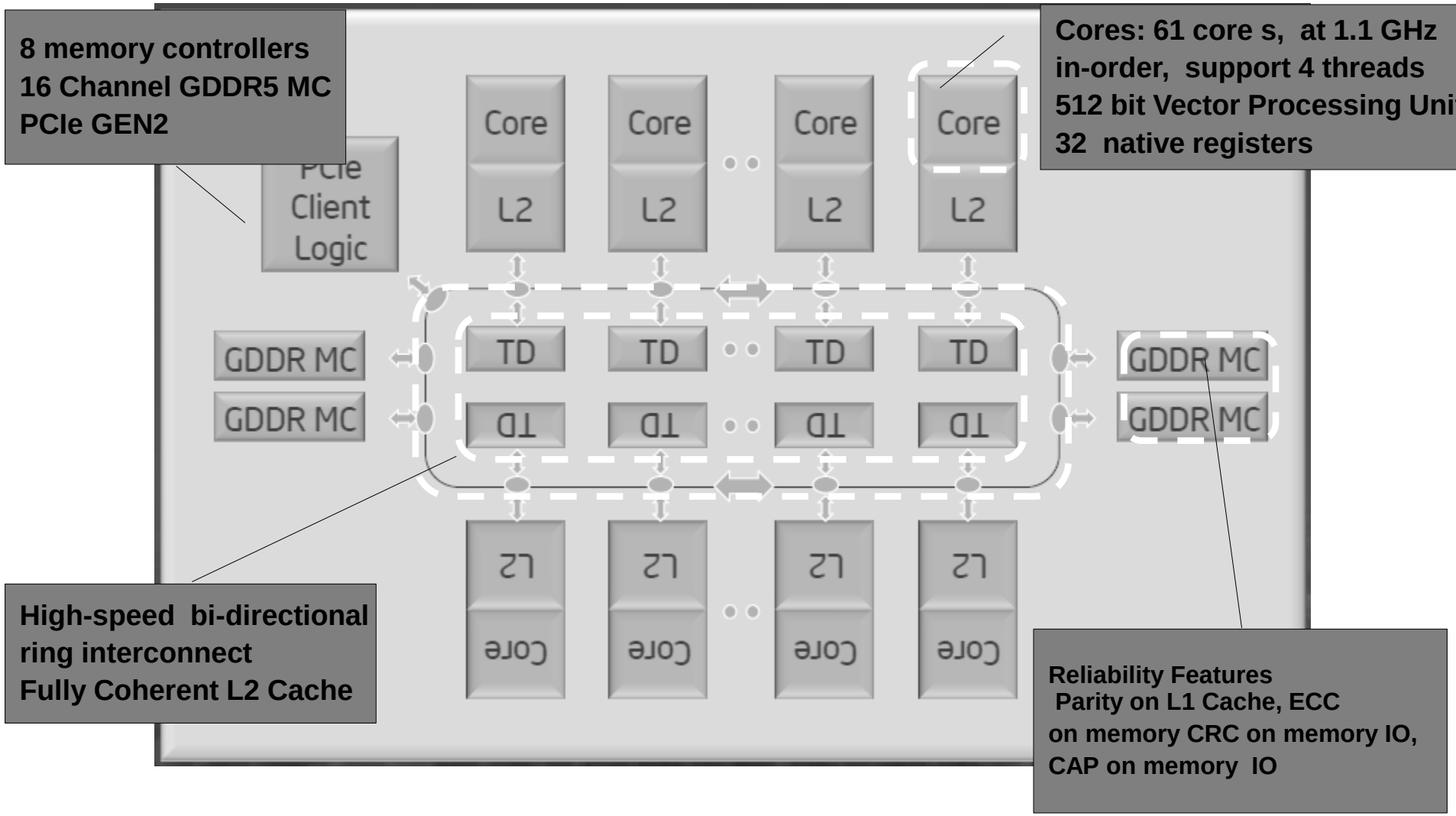
Architecture Overview

An Overview of Computing Scenrario

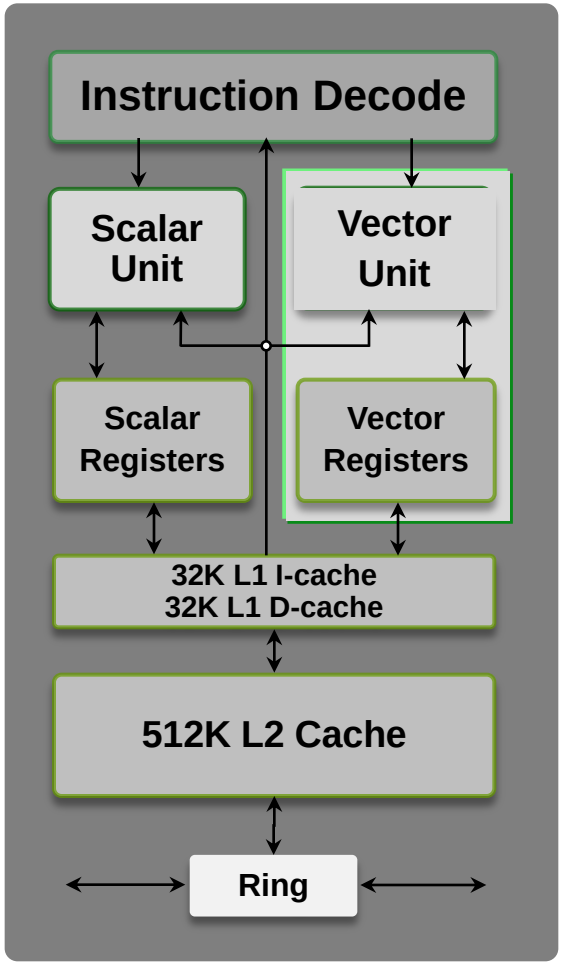


Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel® Xeon Phi™ Architecture Overview



Intel Xeon Phi Core Architecture Overview



- 60+ in-order, low power IA cores in a ring interconnect
- Two pipelines
  - Scalar Unit based on Pentium® processors
  - Dual issue with scalar instructions
  - Pipelined one-per-clock scalar throughput
- SIMD Vector Processing Engine
- 4 hardware threads per core
  - 4 clock latency, hidden by round-robin scheduling of threads
  - Cannot issue back to back inst in same thread
- Coherent 512KB L2 Cache per core

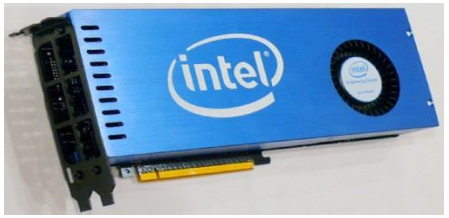
MIC Architecture

- MIC : Many Integrated Core
- Knight Corner co-processor
- Intel Xeon Phi co-processor
  - 22 nm technology
  - > 50 Intel Architecture cores
  - connected by a high performance on-die bi-directional interconnect.
  - I/O Bus: PCIe
  - Memory Type: GDDR5 and >2x bandwidth of KNF
  - Memory size: 8 GB GDDR5 memory technology
  - Peak performance: >1 TFLOP (DP)
  - Single Linux image per chip

Source : References & Intel Xeon-Phi; http://www.intel.com/

(Xeon Phi Hardware)

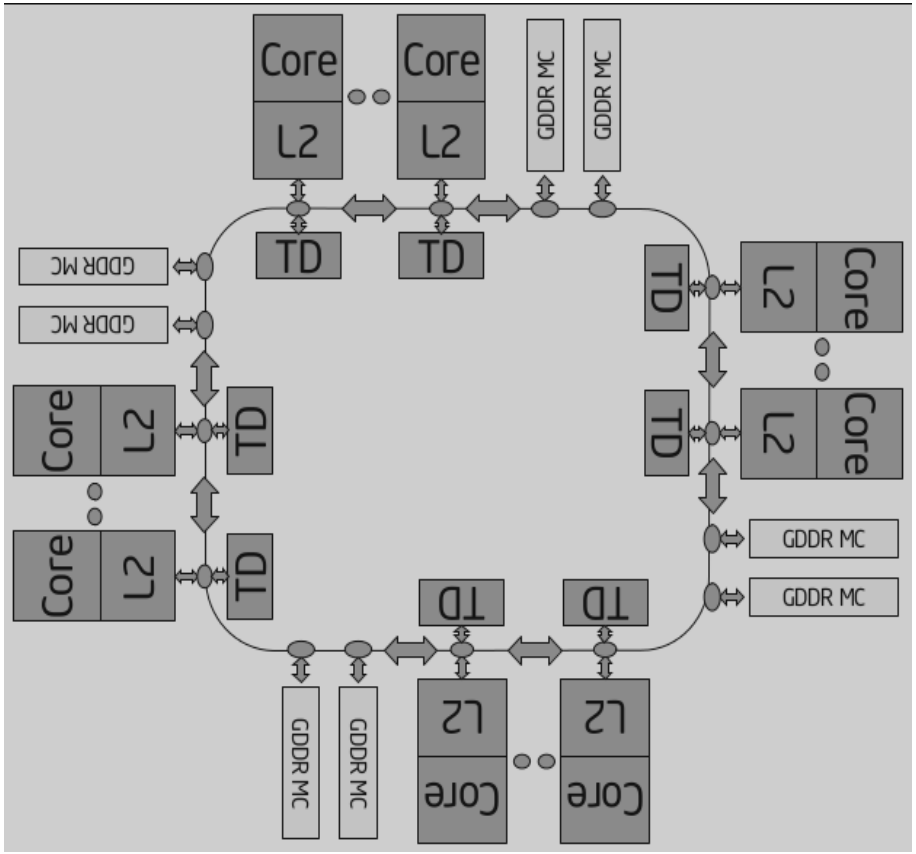
- X16 PCIe 2.0 card in Xeon host system
  - Up to 60 cores, bi-directional ring bus
  - 1-2GB GDDR5 main memory
- CPU cores
  - 1.2GHz, 4-way threading
  - 512-bit SIMD vector unit
  - 32KB L1, 256KB L2



Source : References & Intel Xeon-Phi; http://www.intel.com/

- Xeon-Phi coprocessor capacity 8GB;
  - processor :Xeon Phi 5110P; memory channel interface speed: 5.0 Giga Transfer/ Sec (GT/s); 8 memory controllers, each accessing two memory channels, used on co-processor

MIC Intel Xeon Phi Ring



- Each microprocessor core is a fully functional, in-order core capable of running IA instructions independently of the other cores.
- Hardware multi-threaded cores
- Each core can concurrently run instructions from four processes or threads.
- The Ring Interconnect connecting all the components together on the chip

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel® Xeon Phi™ Coprocessor Arch – System SW Perspective

- Large SMP UMA machine – a set of x86 cores to manage
  - 4 threads and 32KB L1I/D, 512KB L2 per core
  - Supports loadable kernel modules – we'll talk about one today
- Standard Linux kernel from kernel.org
  - 2.6.38 in the most recent release
  - Completely Fair Scheduler (CFS), VM subsystem, File I/O
- Virtual Ethernet driver– supports NFS mounts from Intel® Xeon Phi™ Coprocessor
- New vector register state per thread for Intel® IMCI
  - Supports "Device Not Available" for Lazy save/restore
- Different ABI – uses vector registers for passing floats
  - Still uses the x86_64 ABI for non-float parameter passing (rdi, rsi, rdx ..)

Intel Xeon Phi - Coprocessor :

Usage

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

- Deafault IP addresses ???•?? •?•??? , ???•?? •?•???, etc. are assigned to the attached Intel Xeon Phi coprocessors. The IP addresses of the attached coprocessors can be listed via the traditional **ifconfig** Linux program.

```
hypack-root@mic-0:~> /sbin/ifconfig
```

Further information can be obtained by running the **micinfo** program on the host.

```
hypack-root@mic-0:~>/sudo/opt/intel/mic/bin/micinfo
```

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

```
hypack-root@mic-0:~>/sudo/opt/intel/mic/bin/micinfo
System Info
 Host OS : Linux
 OS Version : 3.0.13-0.27-default
 Driver Version : 4346-16
 MPSS Version : 2.1.4346-16
 Host Physical Memory : 66056 MB
 ……
 Device No: 0, Device Name: Intel(R) Xeon Phi(TM) coprocessor
 ……
 Version
 ……..…
 Board
 …….
```

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

```
hypack-root@mic-0:~>/sudo/opt/intel/mic/bin/micinfo
 Device No: 0, Device Name: Intel(R) Xeon Phi(TM) coprocessor
 ……..
 Core
 ……..…
 Thermal
 ……..
 GGDR
 ……..
 Device No: 1, Device Name: Intel(R) Xeon Phi(TM) coprocessor
 ……..
 ……..
 ……..
```

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

Users can log in directly onto the Xeon Phi coprocessor via ssh. User can get basic information abbot Xeon-Phi by executing the following commands.

```
[hypack01@mic-0]$ ssh mic-0
[hypack01@mic-0]$ hostname
.....
[hypack01@mic-0]$ cat /etc/issue
 Intel MIC Platform Software Stack release 2.1
```

To get further information about the cores, memory etc. can be obtained from the virtual Linux /proc or /sys filesystems:

```
[weinberg@knf1-mic0 weinberg]$
[hypack01@mic-0]$ tail -n26 /proc/cpuinfo
.....
```

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

```
hypack-root@mic-0:~>/sudo/opt/intel/mic/bin/micinfo
 Device No: 0, Device Name: Intel(R) Xeon Phi(TM) coprocessor
 ……..
 Core
 ……..…
```

Intel Xeon Phi Coprocessor : Prog. Env & Performance Issues (In brief)

Intel Xeon-Phi : Shared Address Prog.

- **Rule of thumb :** An application must scale well past one hundred threads on Intel Xeon processors to profit from the possible higher parallel performance offered with e.g. the Intel Xeon Phi coprocessor.

- The scaling would profit from utilising the highly parallel capabilities of the MIC architecture, you should start to create a simple performance graph with a varying number of threads (from one up to the number of cores)

Xeon Phi : Programming Environment

- **Shared Address Space Programming (Offload, Native, Host)**

  OpenMP, Inetl TBB, Cilk Plus, Pthreads

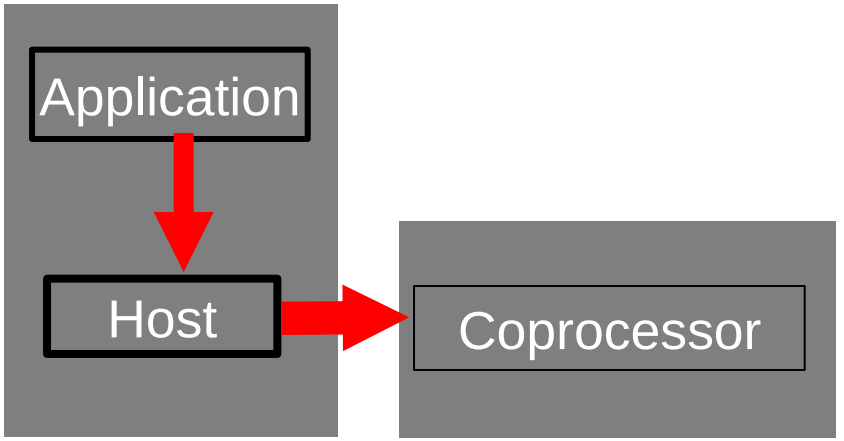
- **Message Passing Programming**

  (Offload – MIC Offload /Host Offload)

  (Symmetric & Coprocessor /Host)

- **Hybrid Programming**

  (MPI – OpenMP, MPI Cilk Plus
  MPI-Intel TBB)



Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi : Shared Address Prog.

- **What we should know from programming point of view :** We treat the coprocessor as a 64-bit x86 **SMP-on-a-chip** with an high-speed bi-directional **ring** interconnect, (up to) **four** hardware threads per core and **512-bit SIMD** instructions.

- With the available number of cores, we have easily 200 hardware threads at hand on a single coprocessor.

Keys to Productive Performance on Intel ® MIC Architecture

- Choose the right Multi-core centric or Many-core centric model for your application
- Vectorize your application (today)
  - Use the Intel vectorizing compiler
- Parallelize your application (today)
  - with MPI (or other multi-process model)
  - With threads (via Intel ® Cilk TM Plus, OpenMP*, Intel ® Threading Building Blocks, Pthreads, etc.)
- Go asynchronous to overlap computation and communication

Source : References & Intel Xeon-Phi; http://www.intel.com/

Programming Challenges

- Alignment with the needs of the business / user / non-computer specialists / community and society
- Need to address the scalability issue: large scale data, high performance computing, automation, response time, rapid prototyping, and rapid time to production
- Need to effectively address (i) ever shortening cycle of obsolescence, (ii) heterogeneity and (iii) rapid changes in requirements
- Transform data from diverse sources into intelligence and deliver intelligence to right people/user/systems
- What about providing all this in a cost-effective manner?

Performance: Intel Xeon-Phi Coprocessor

- Vectorization is key for performance
  - Sandybridge, MIC, etc.
  - Compiler hints
  - Code restructuring
- Many-core nodes present scalability challenges
  - Memory contention
  - Memory size limitations

Source : References & Intel Xeon-Phi; http://www.intel.com/

Optimization Framework

A collection of methodology and tools that enable the developers to express parallelism for Multicore and Manycore Computing

Objective: Turning unoptimized program into a scalable, highly parallel application on multicore and manycore architecture

Step 1: Leverage Optimized Tools, Library

Step 2: Scalar, Serial Optimization /Memory Access

Step 3: Vectorization & Compiler

Step 4: Parallelization

Step 5: Scale from Multicore to Manycore

Source : References & Intel Xeon-Phi; http://www.intel.com/

Porting on MIC

Pros:

- Compilation with an additional Intel compiler flag (`-mmic`);
- Scalability tests: fast and smooth;
- Quick analysis with Intel tools (VtuneT, Itac Intel Trace Analyzer and Collector;
- Porting time: one day with validation of the numerical result;
- expert developer of FARM, with good knowledge of the Intel Compiler, But with only a basic knowledge of MIC.
- Best scalability with OpenMP and Hybrid.

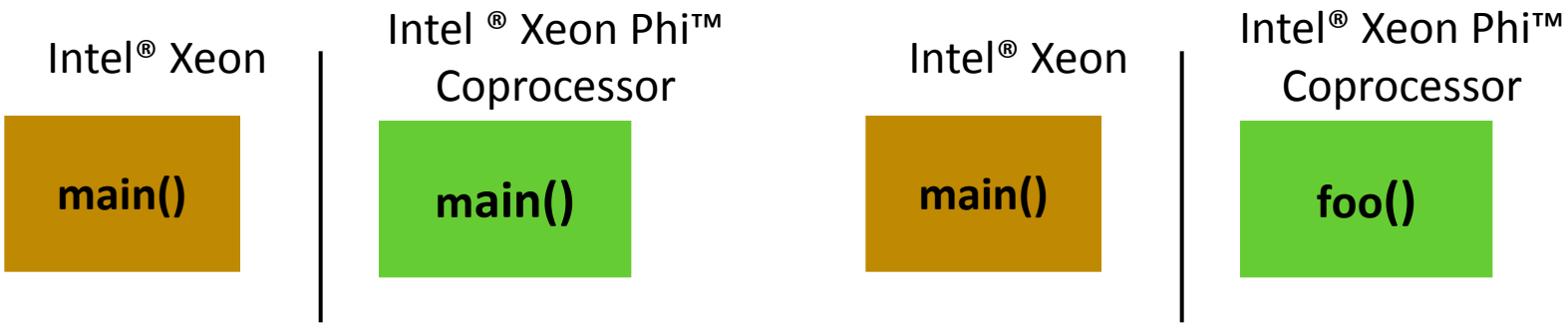
Source : References & Intel Xeon-Phi; http://www.intel.com/

Issues to be addressed

- `MPI Init` routine problem: increasing CPU time for increasing number of processes; Same problem when using two MICs together;
- Detailed analysis of OpenMP threads & thread affinity and Memory available per thread
- Execution time depends strongly from code vectorization, so compiler vectorization for data parallel and task parallel constructs
- code re-structure and memory access pattern are a key point to have a vectorizable satisfactory overall Performances.

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon & Xeon Phi : Execution Modes



Native

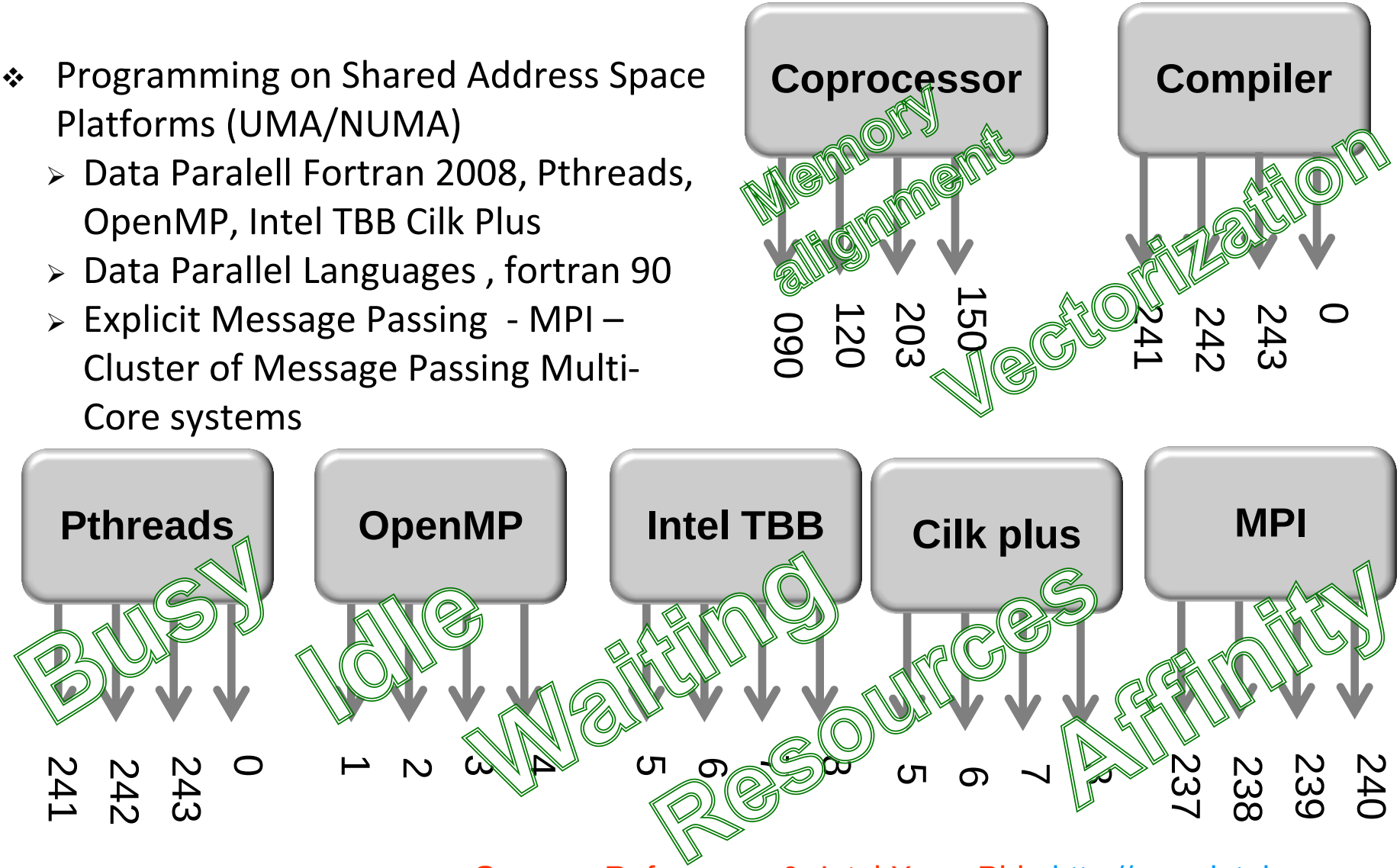
- Card is an SMP machine running Linux
- Separate executables run on both MIC and Xeon
  - e.g. Standalone MPI applications
- No source code modifications most of the time
  - Recompile code for Xeon Phi™ Coprocessor
- Autonomous Compute Node (ACN)

Offload

- "main" runs on Xeon
- Parts of code are offloaded to MIC
- Code that can be
  - Multi-threaded, highly parallel
  - Vectorizable
  - Benefit from large memory BW
- Compiler Assisted vs. Automatic
  - #pragma offload (…)

Intel Xeon –Phi Programming Paradigms

- Programming on Shared Address Space Platforms (UMA/NUMA)
  - Data Paralell Fortran 2008, Pthreads, OpenMP, Intel TBB Cilk Plus
  - Data Parallel Languages , fortran 90
  - Explicit Message Passing - MPI – Cluster of Message Passing Multi-Core systems

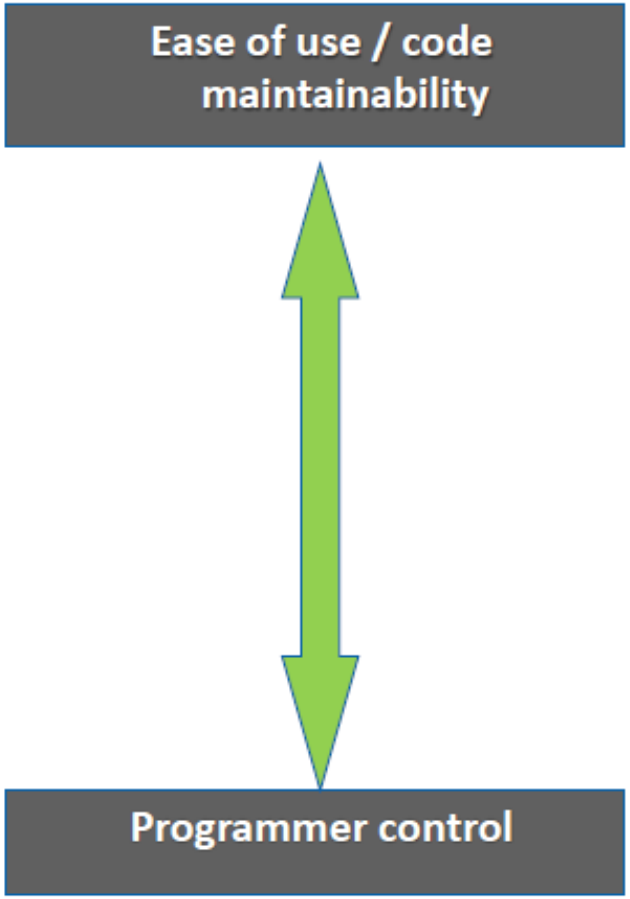


Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi Coprocessor : Prog. Env & Compiler & Vectorization

Options for Thread Parallelism

- Intel® Math Kernel Library
- Intel® Threading Building Blocks
  Intel® Cilk™ Plus
- OpenMP*
- Pthreads* and other threading libraries



Source : References & Intel Xeon-Phi; http://www.intel.com/

Use Compiler Optimization Switches

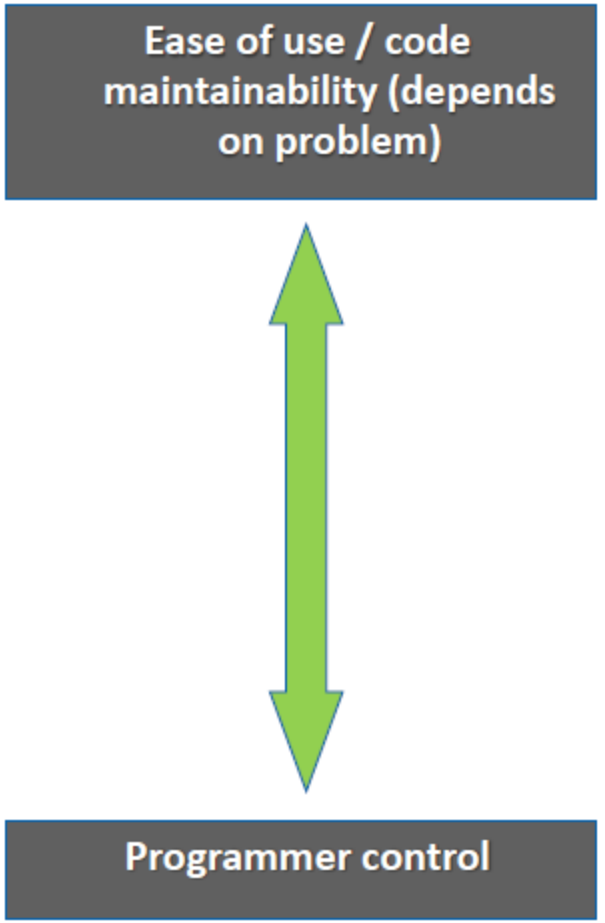
Compiler & Vectorization

Optimization Done	Linux*
Disable optimization	-O0
Optimize for speed (no code size increase)	-O1
Optimize for speed (default)	-O2
High-level loop optimization	-O3
Create symbols for debugging	-g
Multi-file inter-procedural optimization	-ipo
Profile guided optimization (multi-step build)	-prof-gen -prof-use
Optimize for speed across the entire program	-fast (same as: -ipo –O3 -no-prec-div -static -xHost)
OpenMP 3.0 support	-openmp
Automatic parallelization	-parallel

Source : References & Intel Xeon-Phi; http://www.intel.com/

Options for Vectorization

- Intel® Math Kernel Library
- Array Notation: Intel® Cilk™ Plus
- Automatic vectorization
- Semiautomatic vectorization with annotation: `#pragma vector`, `#pragma ivdep`, and `#pragma simd`
- C/C++ Vector Classes (`F32vec16`, `F64vec8`)
- Vector intrinsics (`_mm_add_ps`, `addps`)



Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

❖ Work done – Compiler's Offload

1. When the Intelcompiler encounters an offload pragma, it generates code for both the coprocessor and the host.
2. Code to transfer the data to the coprocessor is automatically created by the compiler,
3. The programmer can influence the data transfer by adding data clauses to the offload pragma.

Details can be found under "**Offload Using a Pragma**" in the Intel compiler documentation.

Offload Code Examples

C/C+ Offload Pragma

```
#pragma offload target (mic)
#pragma omp parallel for reduction(+:pi)
 for (i = 0; i<count; i++) {
      float t = (float) (i+0.5/count);
      pi += 4.0/(1.0t*t);
 }
pi/ = count;
```

C/C++ Offload Pragma

```
#pragma offload target(mic)
      in(transa, transb, N, alpha, beta) \
      in(A:length(matrix_elements)) \
      in(B:length(matrix_elements)) \
      inout(C:length(matrix_elements))
         sgemm(&transa, &transb, &N, &N, &N,
& alpha, A, &N, B, & N, &beta, C &N);
```

Fortran Offload Directives

```
!dir$ omp offload target(mic)
!$omp parallel do
     do i = 1, 10
                A(i) = B(i) * C(i)
     enddo
```

C/C++ Language Extension

```
class_Cilk_Shated common {
    int data1;
    int *data2;
    class common *next;
    void process();
}
_Cilk_Shared class common obj1, obj2;
_Cilk_spawn _offload obj1.process();
_Cilk_spawn  _offload  obj2.process();
```

Source : References & Intel Xeon-Phi; http://www.intel.com/

Options for Parallelism – pthreads*

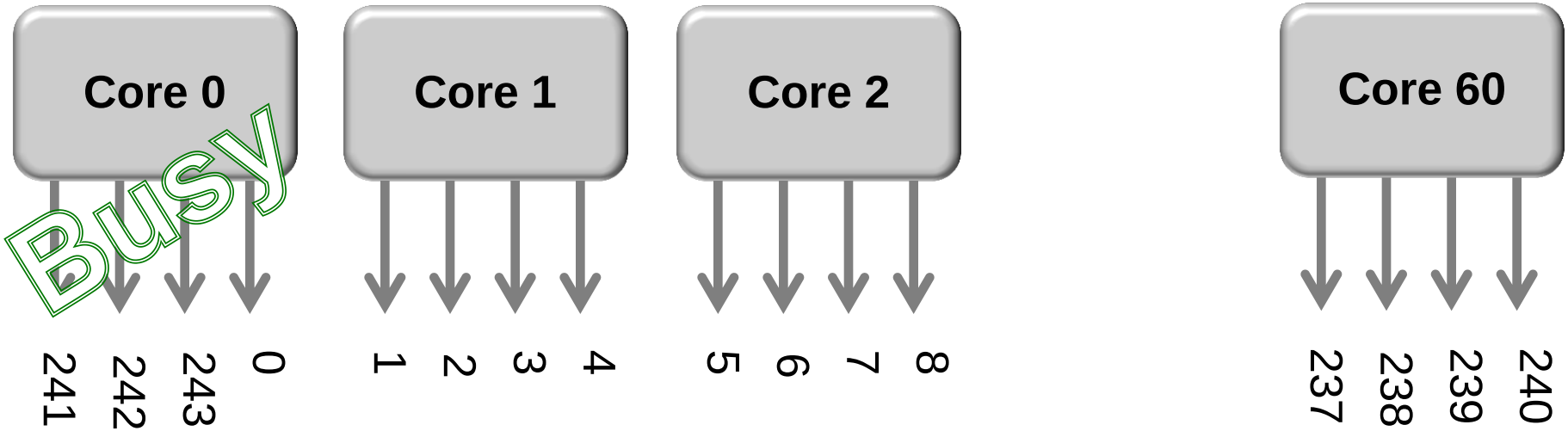
POSIX Threads

- POSIX* Standard for thread API with 20 years history
- Foundation for other high level threading libraries
- Independently exist on the host and Intel® MIC
- No extension to go from the host to Intel® MIC
- Advantage: Programmer has explicit control
  - From workload partition to thread creation, synchronization, load balance, affinity settings, etc.
- Disadvantage: Programmer has too much control
  - Code longevity
  - Maintainability
  - Scalability

Source : References & Intel Xeon-Phi; http://www.intel.com/

Thread Affinity using pthreads*

- Partition the workload to avoid load imbalance
  - Understand static vs. dynamic workload partition
- Use pthread API, define, initialize, set, destroy
  - Set CPU affinity with `pthead_setaffinity_np()`
  - Know the thread enumeration and avoid core 0
  - Core 0 boots the coprocessor, job scheduler, service interrupts



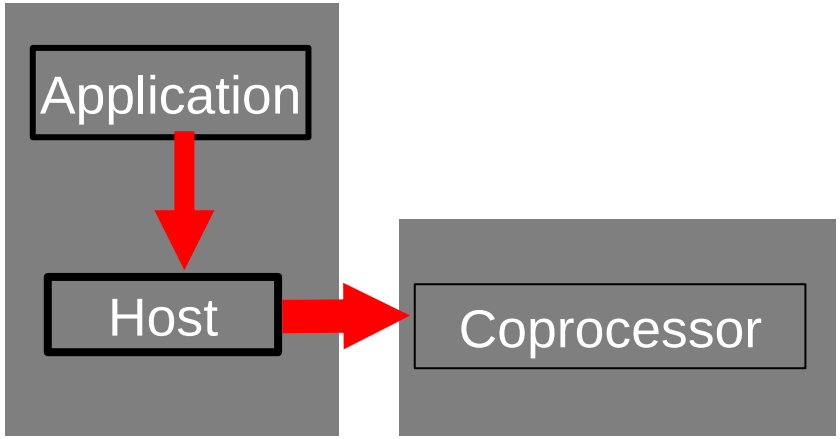
Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi : OpenMP I Prog. Model

OpenMP

- OpenMP parallelization on an "**Intel Xeon + Xeon Phi coprocessor machine**" can be applied in **four** different programming models.

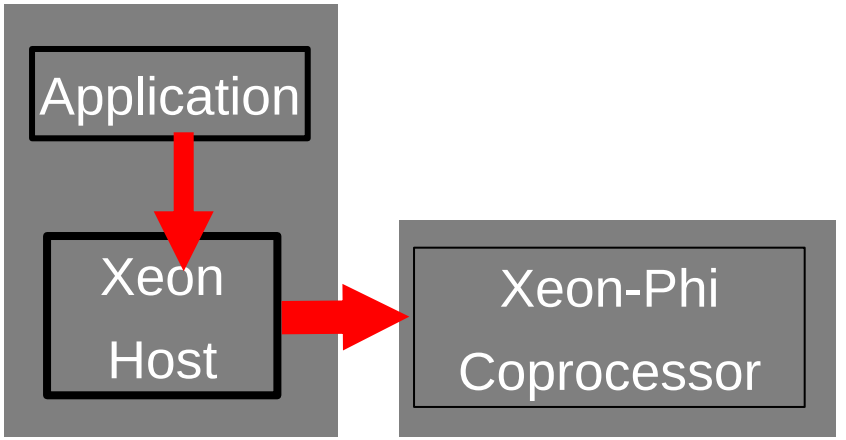
  - **Realized with Complier Options**



Intel Xeon-Phi : OpenMP I Prog. Model

❖ **Four** Models with different programming models

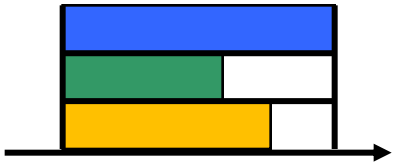
- Native OpenMP on the Xeon host
- Serial Xeon host with OpenMP offload
- Native OpenMP on the Xeon Phi coprocessor
- OpenMP on the Xeon Host with OpenMP offload



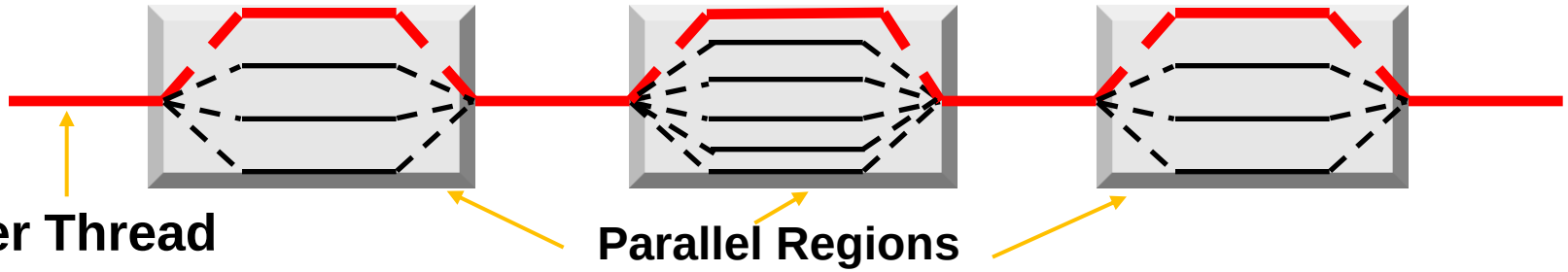
Options for Parallelism – OpenMP*

- Compiler directives/pragmas based threading constructs
  - Utility library functions and Environment variables
- Specify blocks of code executing in parallel

```
#pragma omp parallel sections
{
    #pragma omp section
    task1();
    #pragma omp section
    task2();
    #pragma omp section
    task3();
```



- Fork-Join Parallelism:
  - Master thread spawns a team of worker threads as needed
  - Parallelism grow incrementally

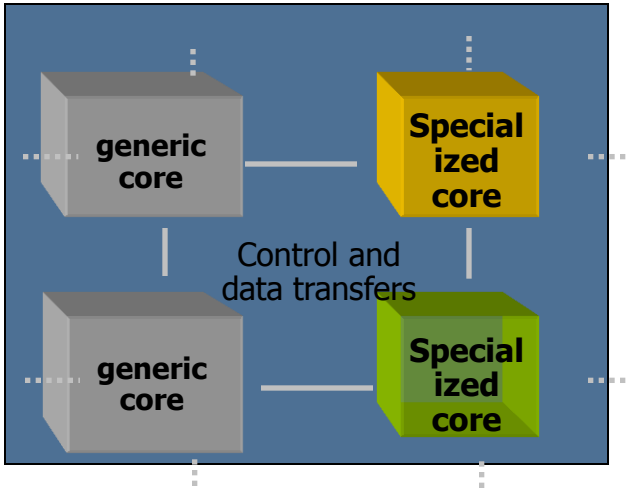


Source : References & Intel Xeon-Phi; http://www.intel.com/

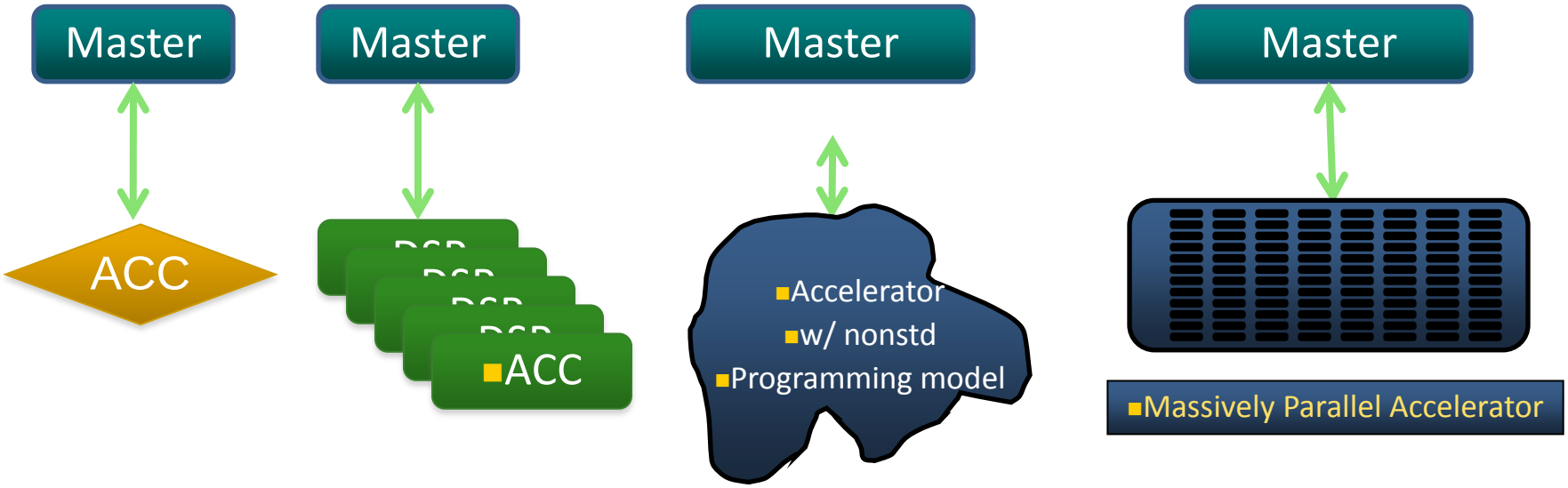
OpenMP Evolution Beyond 1,00,000 cores

- OpenMP language committee is actively working toward the expression of locality and heterogeneity
  - And to improve task model to enhance asynchrony

- How to identify code that should run on a certain kind of core?
- How to share data between host cores and other devices?
- How to minimize data motion?
- How to support diversity of cores?



OpenMP 4.0 Attempts To Target Range of Acceleration Configurations



- Dedicated hardware for specific function(s)
  - ❑ Attached to a master processor
  - ❑ Multiple types or levels of parallelism
    - Process level, thread level, ILP/SIMD
- May not support a full C/C++ or Fortran compiler
  - May lack stack or interrupts, may limit control flow, types

Intel Xeon-Phi Coprocessor : MPI on Cluster

Threading and affinity : Settings :

Settings	Description
OpenMP on host without HT	1 x ncore-host
OpenMP on host with HT	2 x ncore-host
OpenMP on Xeon Phi in native mode	4 x ncore-phi
OpenMP on Xeon Phi in offload mode	1 x ncore-phi-1

- If OpenMP regions exist on the **host** and on the part of the code **offloaded** to the Xeon Phi, **two** separate OpenMP runtimes exist.

Intel® Cilk™ Plus Technology: Elemental Function

Cilk Plus

- Allow you to define data operations using scalar syntax
- Compiler apply the operation to data arrays in parallel, utilizing both SIMD parallelism and core parallelism

Programmer	Build with Intel Cilk Plus Compiler
1. Writes a standard C/C++ scalar syntax 2. Annotate it with **__declspec**(vector) 3. Use one of the parallel syntax choices to invoke the function	1. Generates vector code with SIMD Instr. 2. Invokes the function iteratively, until all elements are processed 3. Execute on a single core, or use the task scheduler, execute on multicores

```
__declspec (vector)
double BlackScholesCall(double S,
                        double K,
                        double T)
                    {
 double d1, d2, sqrtT = sqrt(T);
d1 = (log(S/K)+R*T)/(V*sqrtT)+0.5*V*sqrtT;
            d2 = d1-(V*sqrtT);
 return S*CND(d1) - K*exp(-R*T)*CND(d2);
                    }
```

```
Cilk_for (int i=0; i < NUM_OPTIONS; i++)
     call[i] = BlackScholesCall(SList[i],
                                KList[i],
                                TList[i]);
```

Source : References & Intel Xeon-Phi; http://www.intel.com/

MPI Prog. Models for Xeon systems with MIC

Message Passing : MPI

Offload

- Intel ® MIC Architecture or host CPU as an accelerator

MIC Offload (direct acceleration)	Host Offload (reverse acceleration)
❖ MPI ranks on the host CPU only ❖ Messages into/out of the host CPU ❖ Intel ® MIC Architecture as an accelerator	❖ MPI ranks on the MIC CPU only ❖ Messages into/out of the MIC CPU ❖ Host CPU as an accelerator

MPI

- MPI ranks on several co-processors and/or host nodes
- Messages to/from any core

Co-processor-only	Symmetric
❖ MPI ranks on the MIC CPU only ❖ Messages into/out of the MIC CPU c/o host CPUs ❖ Threading possible	❖ MPI ranks on the MIC and host CPUs ❖ Messages into/ out of the MIC and host CPUs ❖ Threading possible

Source : References & Intel Xeon-Phi; http://www.intel.com/

MKL (Math Kernel Lib.

Simple way to Jobs using Intel MKL (Math Kernel Library)

Details on using MKL (11.0) with Intel Xeon Phi co-processors can be found in references. Also the MKL developer zone contains useful information. Intel MKL 11.0 Update 2 the following functions are highly optimized for the Xeon Phi

- BLAS Level 3, and much of Level 1 & 2
- Sparse BLAS:
- Some important LAPACK routines (LU, QR, Cholesky)
- Fast Fourier Transformations
- Vector Math Library & Other Lib.

Remark : All functions can be used on the Xeon Phi, however the optimization level for wider 512-bit SIMD instructions differs.

Intel Xeon-Phi Coprocessors (Intel MKL)

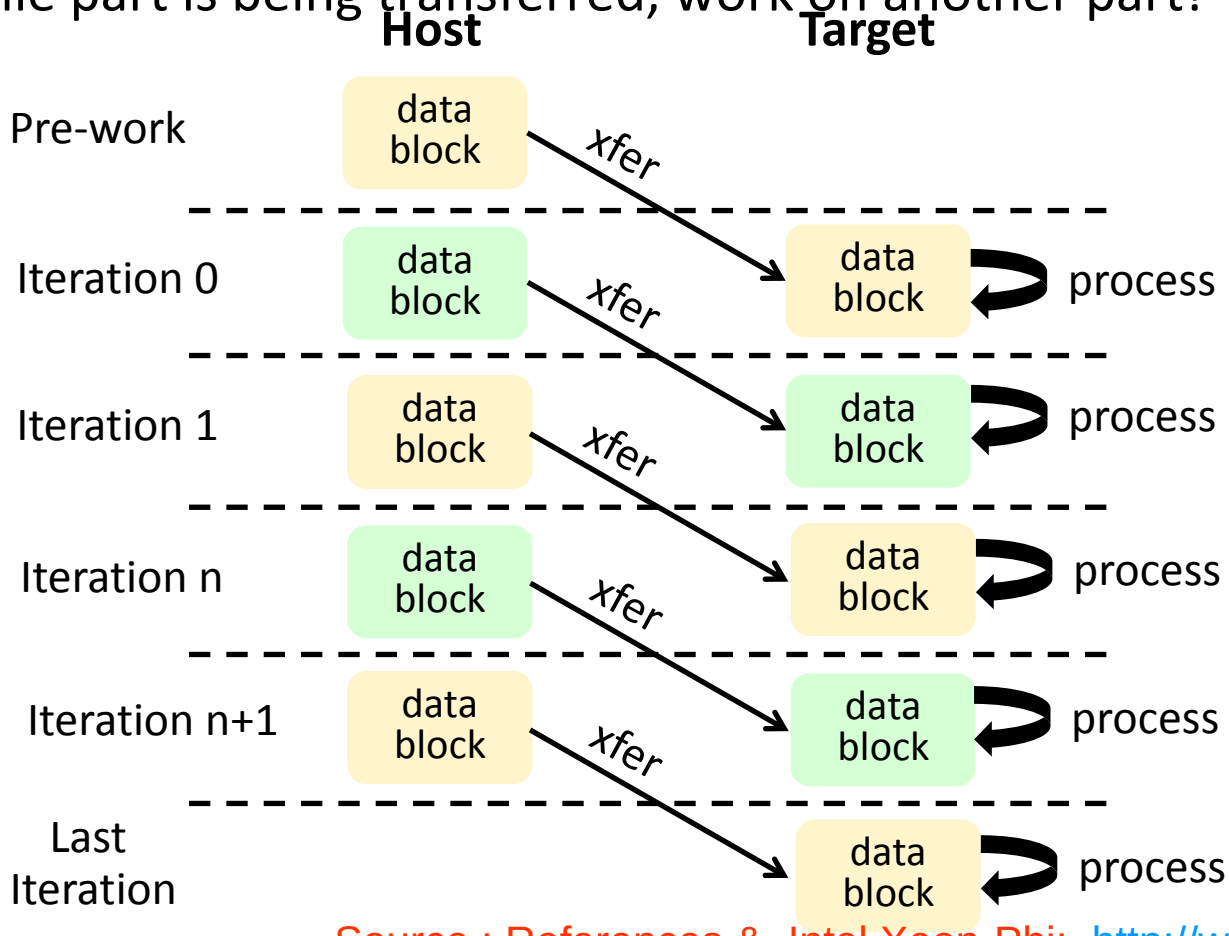
- On Xeon Phi coprocessor, the following usage models of MKL are available :
  - **Automatic Offload**
  - **Compiler Assisted Offload**
  - **Native Execution**

To know more about the availability of various functions for above usage models, Please refer MKL documents

Double Buffering Example

Asynchronous Comp.

- Transfer and work on a dataset in small pieces
- While part is being transferred, work on another part!



Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi Coprocessor : Example Demonstration

Vector-Vector & Matrix-Matrix Addition

Vector-Vector & Matrix-Matrix Multiplication

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Thank You

Any questions ?