C-DAC Four Days Technology Workshop

ON

Hybrid Computing – Coprocessors/Accelerators
Power-Aware Computing – Performance of Applications Kernels

hyPACK-2013

Mode 3 : Intel Xeon Phi Coprocessors

Lecture Topic :

Intel Xeon-Phi Coprocessor An Overview

***Venue** : CMSD, UoHYD ; **Date** : October 15-18, 2013*

An Overview of Xeon Phi Coprocessor

Lecture Outline

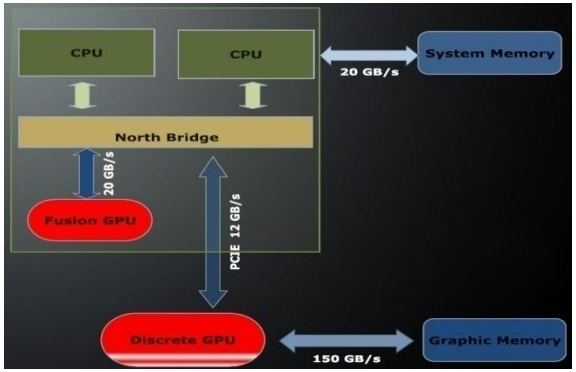
Following topics will be discussed

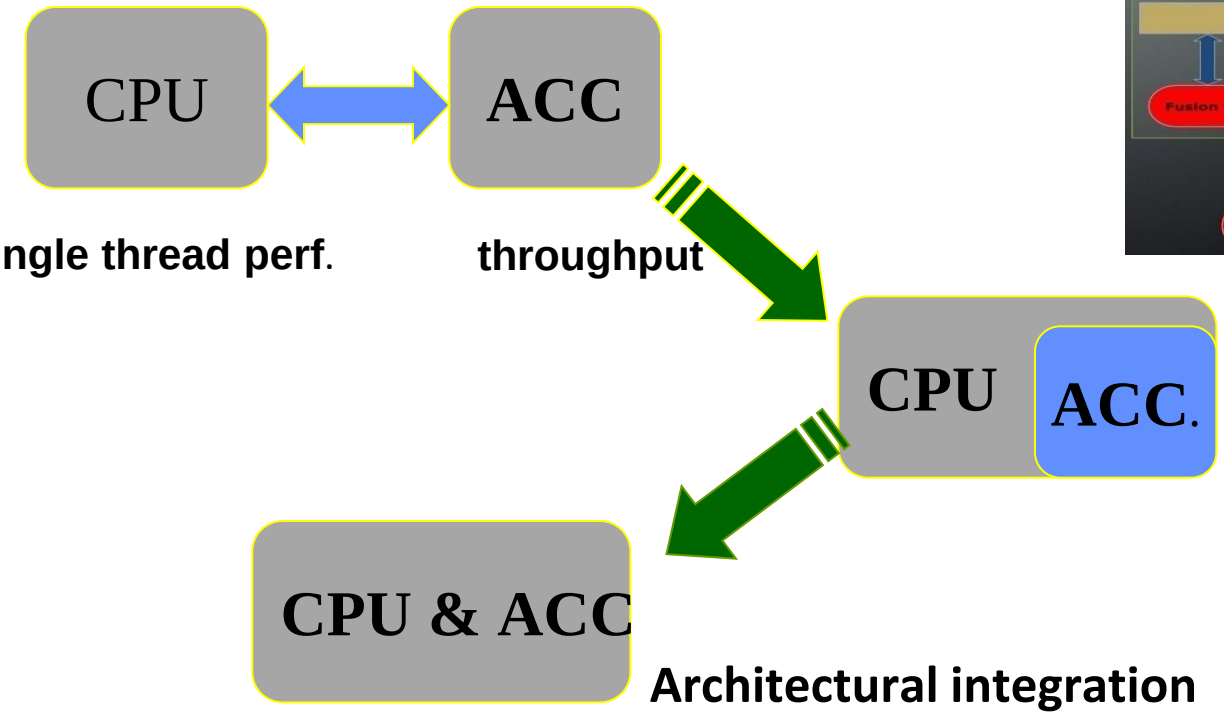
- Understanding of Xeon –Phi Architectures
- Programming Environment on Xeon-Phi Architectures – Compilation
- Tuning & Performance – Compilation & Vectorization

Programming Environment
Compilation
& Performance Issues

Systems with Accelerators

A set (one or more) of very simple execution units that can perform few operations (with respect to standard CPU) with very high efficiency. When combined with full featured CPU (CISC or RISC) can accelerate the “nominal” speed of a system.



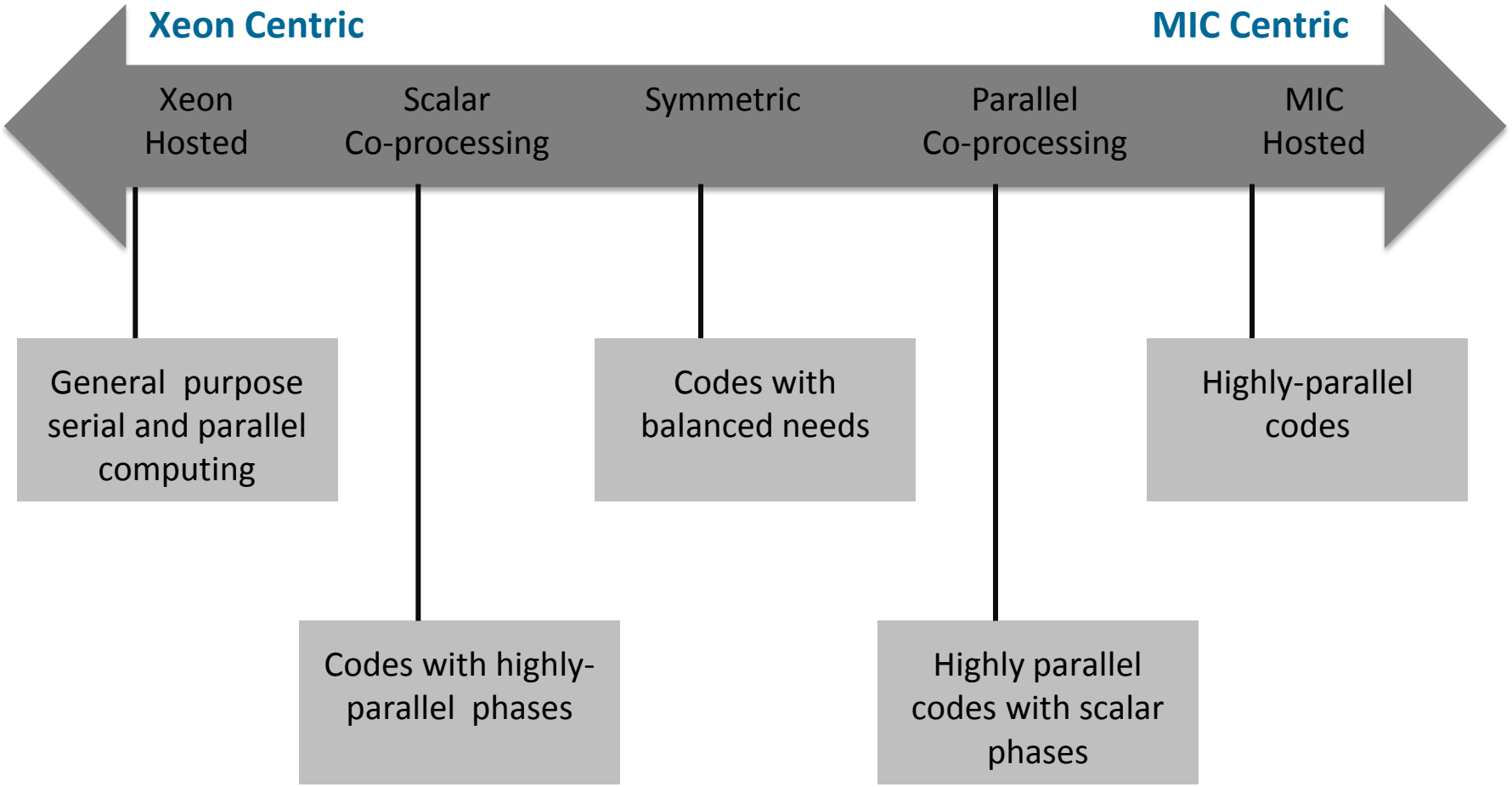


CPU : Control Path & Data Path
ALU : Arithmetic and logic units
ACC: Accumulator
PC : Program counter
Micro-Instructions (Register transfer)

Source : NVIDIA, AMD, SGI, Intel, IBM Alter, Xilinux References

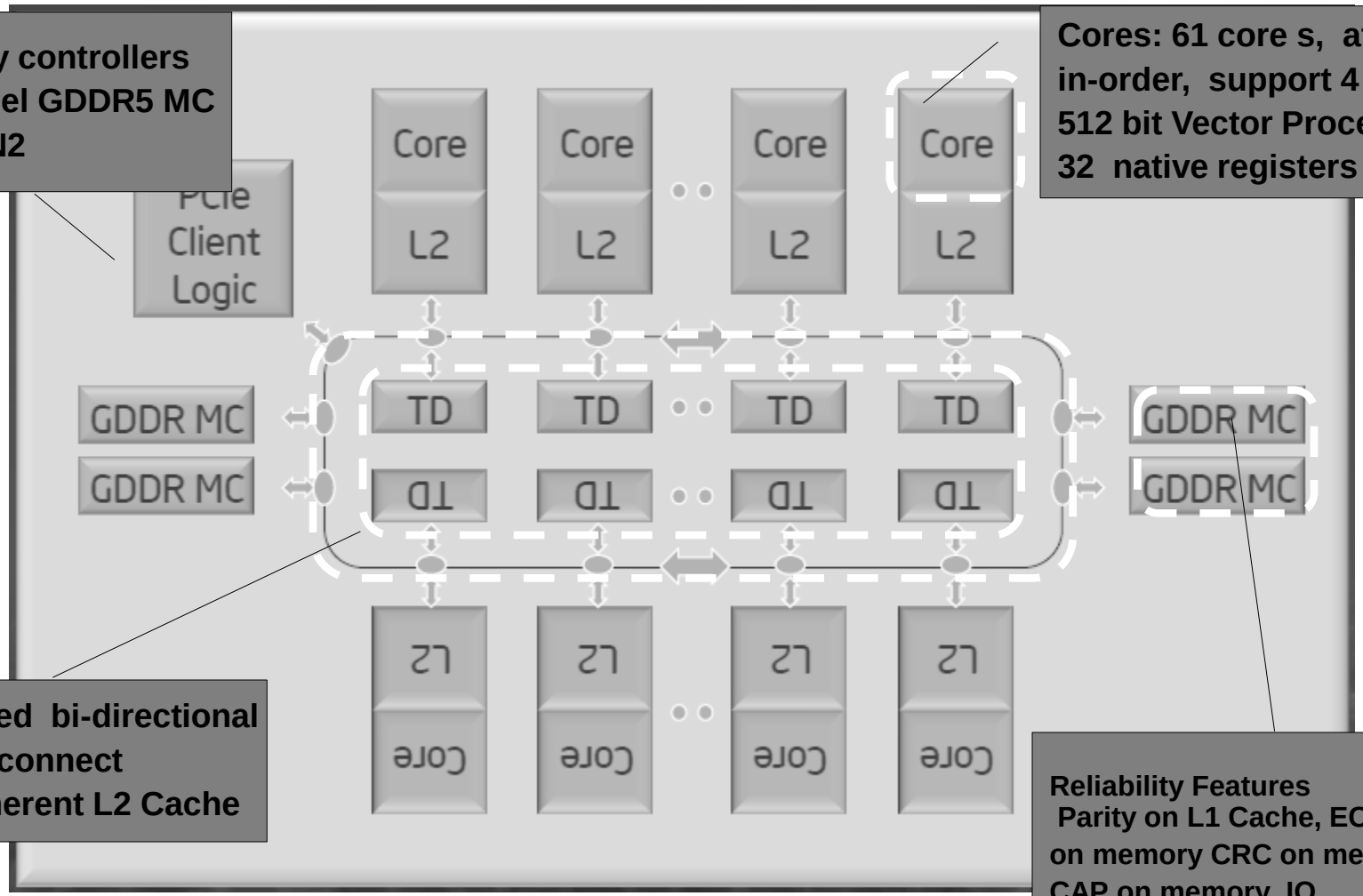
MIC Architecture, System Overview

Compute modes vision



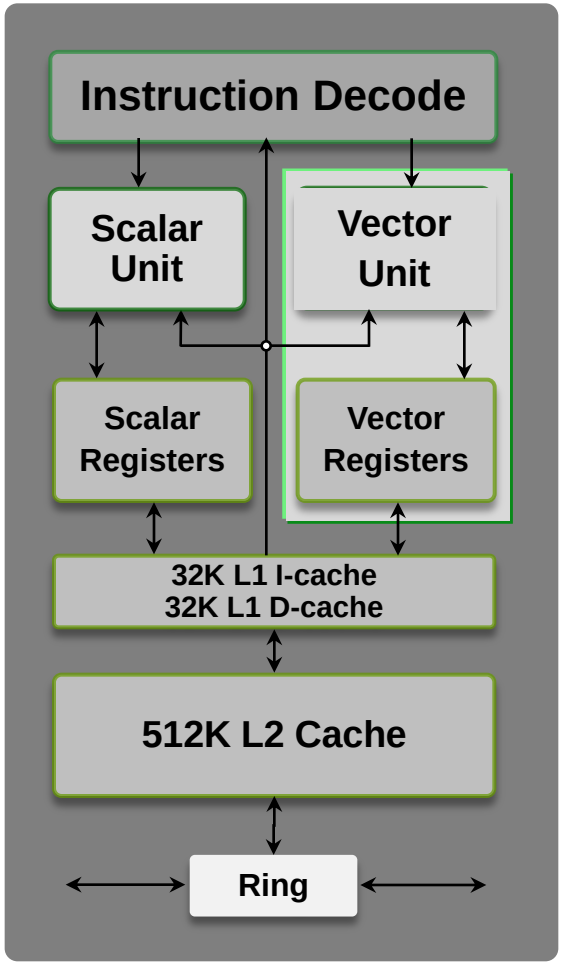
Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel® Xeon Phi™ Architecture Overview



Source : References & Intel Xeon-Phi; http://www.intel.com/

Core Architecture Overview



- 60+ in-order, low power IA cores in a ring interconnect
- Two pipelines
  - Scalar Unit based on Pentium® processors
  - Dual issue with scalar instructions
  - Pipelined one-per-clock scalar throughput
- SIMD Vector Processing Engine
- 4 hardware threads per core
  - 4 clock latency, hidden by round-robin scheduling of threads
  - Cannot issue back to back inst in same thread
- Coherent 512KB L2 Cache per core

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi Coprocessor architecture Overview

Quick Glance*

- The Intel Xeon Phi coprocessor Architecture Overview (Core, VPU, CRI, Ring, SBOX, GBOX, PMU)
- The Cache hierarchy (Details of L1 & L2 Cache)
- Network Configuration (MPSS) : (Obtain the information can be obtained by running the micinfo program on the host.)
- System Access

Remark : Root privileges are necessary for the destination directories (Required for availability of some library usage for codes such MKL)

(= Useful for tuning and Performance)*

Intel Xeon-Phi Coprocessor architecture Overview

- The Intel Xeon Phi coprocessor consists of up to 61 cores connected by a high performance on-die bidirectional interconnect.
- The coprocessor runs a full service Linux operating system
- The coprocessor supports all important Intel development tools, like C/C++ and Fortran compiler, MPI and OpenMP
- To Coprocessor support s high performance libraries like MKL, debugger and tracing tools like Intel VTune Amplifier XE.

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi Coprocessor architecture Overview

- The Intel Xeon Phi coprocessor The coprocessor is connected to an Intel Xeon processor - the "host" - via the PCI Express (PICe) bus.
- The implementation of a virtualized TCP/IP stack allows to access the coprocessor like a network node.

Remark : Summarized information can be found In the following MIC architecture from the System Software Developers Guide and other references

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

- Details about the system startup and the network configuration can be found in Intel Xeon-Phi documentation coming with MPSS
- To start the Intel Manycore Platform Software Stack (Intel MPSS) and initialize the Xeon Phi coprocessor the following command has to be executed as root or during host system start-up:

```
hypack-root@mic-0:~> sudo service mpss start
```

Remark : The above command has to be executed as a root

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

- To start the Intel Manycore Platform Software Stack (Intel MPSS) and initialize the Xeon Phi coprocessor the following command has to be executed as root or during host system start-up:

```
hypack-root@mic-0:~> sudo service mpss start
```

Remark : The above command has to be executed as a root.

Details about the system startup and the network configuration can be found in Intel Xeon-Phi documentation coming with MPSS. For other necessary commands, refer Intel Xeon Phi documentation

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

- Deafault IP addresses ???•?? •?•??? , ???•?? •?•???, etc. are assigned to the attached Intel Xeon Phi coprocessors. The IP addresses of the attached coprocessors can be listed via the traditional **ifconfig** Linux program.

```
hypack-root@mic-0:~> /sbin/ifconfig
```

Further information can be obtained by running the **micinfo** program on the host.

```
hypack-root@mic-0:~>/sudo/opt/intel/mic/bin/micinfo
```

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

```
hypack-root@mic-0:~>/sudo/opt/intel/mic/bin/micinfo
System Info
 Host OS : Linux
 OS Version : 3.0.13-0.27-default
 Driver Version : 4346-16
 MPSS Version : 2.1.4346-16
 Host Physical Memory : 66056 MB
 ……
 Device No: 0, Device Name: Intel(R) Xeon Phi(TM) coprocessor
 ……
 Version
 ……..…
 Board
 …….
```

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

```
hypack-root@mic-0:~>/sudo/opt/intel/mic/bin/micinfo
 Device No: 0, Device Name: Intel(R) Xeon Phi(TM) coprocessor
 ……..
 Core
 ……..…
 Thermal
 ……..
 GGDR
 ……..
 Device No: 1, Device Name: Intel(R) Xeon Phi(TM) coprocessor
 ……..
 ……..
 ……..
```

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

```
hypack-root@mic-0:~>/sudo/opt/intel/mic/bin/micinfo
 Device No: 0, Device Name: Intel(R) Xeon Phi(TM) coprocessor
 ……..
 Core
 ……..…
```

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

Users can log in directly onto the Xeon Phi coprocessor via ssh. User can get basic information abbot Xeon-Phi by executing the following commands.

```
[hypack01@mic-0]$ ssh mic-0
[hypack01@mic-0]$ hostname
.....
[hypack01@mic-0]$ cat /etc/issue
 Intel MIC Platform Software Stack release 2.1
```

To get further information about the cores, memory etc. can be obtained from the virtual Linux /proc or /sys filesystems:

```
[weinberg@knf1-mic0 weinberg]$
[hypack01@mic-0]$ tail -n26 /proc/cpuinfo
.....
```

Intel Xeon-Phi : Performance-Tips

Performance on Xeon Phi using different prog.

- **Rule of thumb :** An application must scale well past one hundred threads on Intel Xeon processors to profit from the possible higher parallel performance offered with e.g. the Intel Xeon Phi coprocessor.

- The scaling would profit from utilising the highly parallel capabilities of the MIC architecture, you should start to create a simple performance graph with a varying number of threads (from one up to the number of cores)

Intel Xeon-Phi : Performance-Tips

Performance on Xeon Phi using different prog.

- **What we should know from programming point of view :** We treat the coprocessor as a 64-bit x86 **SMP-on-a-chip** with an high-speed bi-directional **ring** interconnect, (up to) **four** hardware threads per core and **512-bit SIMD** instructions.

- With the available number of cores, we have easily 200 hardware threads at hand on a single coprocessor.

Intel Xeon System & Xeon-Phi

Performance on Xeon Phi using different prog.

About Hyper-Threading

- hyper-threading hardware threads can be switched off and can be ignored.

About Threading on Xeon-Phi Coprocessor

- The multi-threading on each core is primarily used to hide latencies that come implicitly with an in-order microarchitecture. Unlike hyper-threading these hardware threads cannot be switched off and should never be ignored.
- In general a minimum of **three** or **four** active threads per cores will be needed.

Programming Environment
Native Compilation
& Intel Complier Offload Pragmas

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

- In native mode an application is compiled on the host using the compiler switch **-mmic** to generate code for the MIC architecture. The binary can then be copied to the coprocessor and has to be started there.
- Vector-Vector-Multiplication

```
[hypack01@mic-0]$ icc -O3 -mmic vv.c -o vv
[hypack01@mic-0]$ scp vv mic0:
    program 100% 10KB 10.2KB/s 00:00
[hypack01@mic-0]$ ssh mic0 ~/run
      vector-vector Multiplication = 16.00
```

Intel Xeon-Phi Coprocessor System Access

Quick Glance:

In native mode an application is compiled on the host using the compiler switch **-mmic** to generate code for

the MIC architecture. The binary can then be copied to the coprocessor and has to be started there.

```
[hypack01@mic-0]$ icc -O3 -mmic test.c -o test

[hypack01@mic-0]$ scp test mic0:
    program 100% 10KB 10.2KB/s 00:00

[hypack01@mic-0]$ ssh mic0 ~/test
                  hello world
```

Intel Xeon Phi Coprocessor :Native Compilation

To achieve good Performance - Following information should be kept in mind.

- Data should be **aligned to 64 Bytes (512 Bits)** for the MIC architecture, in contrast to 32 Bytes (256 Bits) for AVX and 16 Bytes (128 Bits) for SSE.
- Due to the large SIMD width of 64 Bytes **vectorization is even more important for the MIC architecture than for Intel Xeon!**
- The MIC architecture offers **new instructions** like
  - **gather/scatter,**
  - **fused multiply-add,**
  - **masked vector instructions etc.**

  which allow more loops to be parallelized on the coprocessor than on an **Intel Xeon based host**.

Intel Xeon Phi Coprocessor : Native Compilation

To achieve good Performance - Following information should be kept in mind.

Use pragmas like

- `#pragma ivdep,`
- `#pragma vector always,`
- `#pragma vector aligned,`
- `#pragma simd`

etc. to achieve autovectorization.

Autovectorization is enabled at default optimization level `-O2`. Requirements for vectorizable loops can be found references.

Intel Xeon Phi Coprocessor : Native Compilation

To achieve good Performance - Following information should be kept in mind.

- Let the compiler generate vectorization reports using the compiler option **`-vecreport2`** to see if loops were vectorized for MIC (Message "*MIC* Loop was vectorized" etc).

- The options –**`opt-report-phase hlo`** (High Level Optimizer Report) or

  –**`opt-report-phase ipo_inl`** (*Inlining* report) may also be useful.

Intel Xeon Phi Coprocessor :Native Compilation

To achieve good Performance - Following information should be kept in mind.

- Explicit vector programming is also possible via Intel Cilk Plus language extensions (C/C++ array notation, vector elemental functions, ...) or the new SIMD constructs from OpenMP 4.0 RC1.
- Vector elemental functions can be declared by using `__attributes__((vector))`. The compiler then generates a vectorized version of a scalar function which can be called from a vectorized loop.

Intel Xeon Phi Coprocessor : Native Compilation

To achieve good Performance - Following information should be kept in mind.

- One can use intrinsics to have full control over the vector registers and the instruction set.
- Include `<immintrin.h>` for using intrinsics.
- **Hardware prefetching** from the L2 cache is enabled per default.
- In addition, **software prefetching** is on by default at compiler optimization level `-O2` and above. Since Intel Xeon Phi is an `inorder` architecture, care about prefetching is more important than on `out-of-order` architectures.

Intel Xeon Phi Coprocessor : Native Compilation

To achieve good Performance - Following information should be kept in mind.

- The compiler prefetching can be influenced by setting the compiler switch **`-opt-prefetch = n`**.

- Manual prefetching can be done by using intrinsics **`(_mm_prefetch`**`()` or

  pragmas (#**`pragma prefetch var`**).

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

- Simply add OpenMP-like pragmas to C/C++ or Fortran code to mark regions of code that should be offloaded to the Intel Xeon Phi Coprocessor and be run there.

- This approach is quite similar to the accelerator pragmas introduced by the

  - NVIDIA - PGI compiler,
  - CAPS HMPP or
  - OpenACC to offload code to GPGPUs.

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

❖ Work done – Compiler's Offload

1. When the Intelcompiler encounters an offload pragma, it generates code for both the coprocessor and the host.
2. Code to transfer the data to the coprocessor is automatically created by the compiler,
3. The programmer can influence the data transfer by adding data clauses to the offload pragma.

Details can be found under "**Offload Using a Pragma**" in the Intel compiler documentation.

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

A simple example how to offload a **matrix-matrix computation** to the coprocessor. (*No function or subroutine) is included*

```
main(){
  double *a, *b, *c;
  int i,j,k, ok, n=100;

  // allocated memory on the heap aligned to 64 byte boundary
  ok = posix_memalign((void**)&a, 64, n*n*sizeof(double));
  ok = posix_memalign((void**)&b, 64, n*n*sizeof(double));
  ok = posix_memalign((void**)&c, 64, n*n*sizeof(double));

// initialize matrices
  ...
```

Code "***Simple example for matrix-matrix computation***" – may not give good performance on all cores

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

```
//offload code
#pragma offload target(mic) in(a,b:length(n*n))
inout(c:length(n*n))
{
//parallelize via OpenMP on MIC
#pragma omp parallel for
  for( i = 0; i < n; i++ ) {
    for( k = 0; k < n; k++ ) {
#pragma vector aligned
#pragma ivdep
 for( j = 0; j < n; j++ ) {
   //c[i][j] = c[i][j] + a[i][k]*b[k][j];
     c[i*n+j] = c[i*n+j] + a[i*n+k]*b[k*n+j];
         }
       }
     }
   }
}
```

Code "***Simple example for matrix-matrix computation***" – may not give good performance on all cores

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Summary of Example Program

1. Shows how to offload the matrix computation to the coprocessor using the `#pragma offload target(mic)`.

2. One could also specify the specific coprocessor `num` in a system with multiple coprocessors by using `#pragma offload target(mic:num)`

3. Matrices have been dynamically allocated using `posix_memalign()`, their sizes must be specified via the `length()` clause.

   It is recommended that for Intel Xeon Phi data is 64-byte aligned

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Summary of Example Program

1. Shows how to offload the matrix computation to the coprocessor using the `#pragma offload target(mic)`.

1. `#pragma vector aligned` tells the compiler that all array data accessed in the loop is properly aligned.

2. `#pragma ivdep` discards any data dependencies assumed by the compiler

Offloading is enabled per default for the Intel compiler. Use `-no-offload` to disable the generation of offload code.

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Obtain Offload Information about the following

Using the compiler option **-vec-report2,** one can see which loops have been vectorized on the host & the MIC coprocessor:

```
[hypack01@mic-0]$ icc -vec-report2 -openmp offload.c

offload.c(57): (col. 2) remark: loop was not vectorized:
           vectorization possible but seems inefficient.

...
offload.c(57):(col. 2) remark: *MIC* LOOP WAS VECTORIZED.
offload.c(54):(col. 7) remark: *MIC* loop was not
                  vectorized: not inner loop.
offload.c(53): (col. 5) remark: *MIC* loop was not
                  vectorized: not inner loop.
```

Mind the **C99** restrict keyword that specifies that the vectors do not overlap. (Compile with **-std=c99**)

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Obtain Offload Information about the following

By setting the environment variable **OFFLOAD_REPORT** one can obtain information about per.& data transfers at runtime:

```
[hypack01@mic-0]$ export OFFLOAD_REPORT=2
[hypack01@mic-0]$ ./a.out
[Offload] [MIC 0] [File] offload2.c
[Offload] [MIC 0] [Line] 50
[Offload] [MIC 0] [CPU Time] 12.853562 (seconds)
[Offload] [MIC 0] [CPU->MIC Data] 9830416 (bytes)
[Offload] [MIC 0] [MIC Time] 12.208636 (seconds)
[Offload] [MIC 0] [MIC->CPU Data] 3276816 (bytes)
offload.c(53): (col. 5) remark: *MIC* loop was not
                vectorized: not inner loop.
```

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

A simple example how to offload a **matrix-matrix computation** to the coprocessor. (*No function or subroutine) is included*

If a function is called within the offloaded code block, this function has to be declared with

```
__attribute__((target(mic)))
```

to disable the generation of offload code.

Code " ***Simple example for matrix-matrix computation***" – may not give good performance on all cores

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

A simple example how to offload a **matrix-matrix computation** a *subroutine and call that routine within an offloaded block region:*

```
attribute__((target(mic))) void mxm( int n, \
      double *restrict a, double * restrict b, \
      double *restrict c ){
   int i,j,k;
   for( i = 0; i < n; i++ ) {
   ...
}
main(){
...
#pragma offload target(mic) \
     in(a,b:length(n*n)) inout(c:length(n*n))
  {
   mxm(n,a,b,c);
  }
}
```

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Syntax of Programs

Pragma	Syntax	Semantic
	C++	
Offload pragma	`#pragma offload <clauses> <statement>`	Allow next statement to execute on coprocessor or host CPU
Variable/function offload properties	`__attribute__ ((target(mic)))`	Compile function for, or allocate variable on, both host CPU and coprocessor
Entire blocks of data/code defs	`#pragma offload_attribute(push, target(mic)) ... #pragma offload_attribute(pop)`	Mark entire files or large blocks of code to compile for both host CPU and coprocessor

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Syntax of Programs

Pragma	Syntax	Semantic
Fortran		
Offload directive	`!dir$ omp offload <clauses> <statement>`	Execute OpenMP parallel block on coprocessor
Variable/function offload properties	`!dir$ attributes offload:<mic> :: <ret-name> OR <var1,var2,…>`	Compile function or variable for CPU and coprocessor
Entire code blocks	`!dir$ offload begin <clauses> ... !dir$ end offload`	Mark entire files or large blocks of code to compile for both host CPU and coprocessor

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Syntax of Programs

The following clauses can be used to control data transfers:

Clause	Syntax	Semantic
Multiple coprocessors	`target(mic[:unit])`	Select specific coprocessors
Inputs	`in(var-list modifiers)`	Copy from host to coprocessor
Outputs	`out(var-list modifiers)`	Copy from coprocessor to host
Inputs & Outputs	`inout(var-list modifiers)`	Copy host to coprocessor and back when offload completes
Non-copied data	`nocopy(var-list modifiers)`	Data is local to target

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Syntax of Programs

The following (optional) modifiers are specified:

Modifier	Syntax	Semantic
Specify copy length	`length(N)`	Copy N elements of pointer's type
Coprocessor memory allocation	`alloc_if ( bool )`	Allocate coprocessor space on this offload (default: TRUE)
Coprocessor memory release	`free_if ( bool )`	Free coprocessor space at the end of this offload (default: TRUE)
Control target data alignment	`align ( N bytes )`	Specify minimum memory alignment on coprocessor
Array partial allocation & variable relocation	`alloc (array-slice ) into ( var-expr )`	Enables partial array allocation and data copy into other vars & ranges

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Explicit Worksharing

```
#pragma omp parallel
  {
#pragma omp sections
    {
#pragma omp section
     {
//section running on the coprocessor
#pragma offload target(mic) in(a,b:length(n*n)) inout(c:length(n*n))
 {
   mxm(n,a,b,c);
 }
      }
#pragma omp section
      {
//section running on the host
mxm(n,d,e,f);
      }
   }
}
```

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Persistent data on the coprocessor

- The main bottleneck of accelerator based programming are data transfers over the slow PCIe bus from the **host** to the accelerator and vice versa.
- To increase the performance one should minimize data transfers as much as possible and keep the data on the coprocessor between computations using the same data.
- Defining the following macros

```
#define ALLOC alloc_if(1)
#define FREE free_if(1)
#define RETAIN free_if(0)
#define REUSE alloc_if(0)
```

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Persistent data on the coprocessor

- The main bottleneck of accelerator based programming are data transfers over the slow PCIe bus from the **host** to the accelerator and vice versa.
- one can simply use the following notation: to allocate data and keep it for the next offload

```
#pragma offload target(mic)in (p:length(l) ALLOC RETAIN)
```

- to reuse the data and still keep it on the coprocessor

```
#pragma offload target(mic)in (p:length(l) REUSE RETAIN)
```

- to reuse the data again and free the memory. (`FREE` is the default, and does not need to be explicitly specified)

```
#pragma offload target(mic) in (p:length(l) REUSE FREE)
```

More information can be found in the section "Managing Memory Allocation for Pointer Variables" under "Offload Using a Pragma"

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Optimised Offloaded Code

- Optimizing offloaded code
- The implementation of the matrix-matrix multiplication can be optimized by defining appropriate ROWCHUNK and COLCHUNK chunk sizes.
- Rewrite the code with 6 nested loops (using OpenMP col-apse for the 2 outermost loops) and some manual loop unrolling

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Optimizing Offloaded Code

```
#define ROWCHUNK 96
#define COLCHUNK 96
#pragma omp parallel for collapse(2) private(i,j,k)
  for(i = 0; i < n; i+=ROWCHUNK ) {
    for(j = 0; j < n; j+=ROWCHUNK ) {
 for(k = 0; k < n; k+=COLCHUNK ) {
  for (ii = i; ii < i+ROWCHUNK; ii+=6) {
   for (kk = k; kk < k+COLCHUNK; kk++ ) {
#pragma ivdep
#pragma vector aligned
       for ( jj = j; jj < j+ROWCHUNK; jj++){
  c[(ii*n)+jj] += a[(ii*n)+kk]*b[kk*n+jj];
  c[((ii+1)*n)+jj] += a[((ii+1)*n)+kk]*b[kk*n+jj];
  c[((ii+2)*n)+jj] += a[((ii+2)*n)+kk]*b[kk*n+jj];
  c[((ii+3)*n)+jj] += a[((ii+3)*n)+kk]*b[kk*n+jj];
  c[((ii+4)*n)+jj] += a[((ii+4)*n)+kk]*b[kk*n+jj];
  c[((ii+5)*n)+jj] += a[((ii+5)*n)+kk]*b[kk*n+jj];
                }
              }
            }
          }
      }
    }
}
```

Intel Xeon Phi : Coprocessors – Intel Compiler's Offload Programs

Optimised Offloaded Code

Tuning & Performance :

- Using intrinsics with manual data prefetching and register blocking can still considerably increase the performance.

- Try to get a suitable vectorization and write cache and register efficient code, i.e. values stored in registers should be reused as often as possible in order to avoid cache and memory access.

Intel Xeon-Phi Compilation & Vectorization

Use Compiler Optimization Switches

Optimization Done	Linux*
Disable optimization	-O0
Optimize for speed (no code size increase)	-O1
Optimize for speed (default)	-O2
High-level loop optimization	-O3
Create symbols for debugging	-g
Multi-file inter-procedural optimization	-ipo
Profile guided optimization (multi-step build)	-prof-gen -prof-use
Optimize for speed across the entire program	-fast (same as: -ipo –O3 -no-prec-div -static -xHost)
OpenMP 3.0 support	-openmp
Automatic parallelization	-parallel

Source : References & Intel Xeon-Phi; http://www.intel.com/

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Compiler Reports – Optimization Report

Compiler switch:

`-opt-report-phase[=phase]`

`phase` can be:

- **`ipo_inl`** - Interprocedural Optimization Inlining Report
- **`ilo`** — Intermediate Language Scalar Optimization
- **`hpo`** — High Performance Optimization
- **`hlo`** — High-level Optimization
- **`all`** — All optimizations (not recommended, output too verbose)

Control the level of detail in the report:

`-opt-report[0|1|2|3]`

If you do not specify the option, no optimization report is being generated; if you do not specify the level (i.e. -opt-report) level 2 is being used by the compiler.

Source : References & Intel Xeon-Phi; http://www.intel.com/

Hints to Compiler for Vectorization

#pragma	Semantics
#pragma ivdep	Ignore vector dependences unless they are proven by the compiler
#pragma vector always [assert]	If the loop is vectorizable, ignore any benefit analysis If the loop did not vectorize, give a compile-time error message via assert
#pragma novector	Specifies that a loop should never be vectorized, even if it is legal to do so, when avoiding vectorization of a loop is desirable (when vectorization results in a performance regression)
#pragma vector aligned / unaligned	instructs the compiler to use aligned (unaligned) data movement instructions for all array references when vectorizing
#pragma vector temporal / nontemporal	directs the compiler to use temporal/non-temporal (that is, streaming) stores on systems based on IA-32 and Intel® 64 architectures; optionally takes a comma separated list of variables

Source : References & Intel Xeon-Phi; http://www.intel.com/

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Get Your Code Vectorized by Intel Compiler

- Data Layout, AOS -> SOA
- Data Alignment (next slide)
- Make the loop innermost
- Function call in treatment
  - Inline yourself
  - inline! Use `__forceinline`
  - Define your own vector version
  - Call vector math library - SVML
- Adopt jumpless algorithm
- Read/Write is OK if it's continuous
- Loop carried dependency

Array of Structures		
S0	X0	T0
S1	X1	T1
…	…	…

Structure of Arrays		
S0	S1	…
X0	X1	…
S0	S1	…

Not a true dependency

```
for(int i = TIMESTEPS; i > 0; i--)
        #pragma simd
        #pragma unroll(4)
  for(int j = 0; j <= i - 1; j++)
cell[j]=puXDf*cell[j+1]+pdXDf*cell[j];
CallResult[opt] = (Basetype)cell[0];
```

A true dependency

```
for (j=1; j<MAX; j++)
a[j] = a[j] + c * a[j-n];
```

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi : Coprocessors – Native Compilation
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Compiler VECreport

- Indicates whether each loop is vectorized
  - Vectorized ≠ efficient
- Different levels
  - -vec-report1, for high-level triage of large code
  - -vec-report2, when you want reasons for not vectorizing
  - -vec-report6, for even more detail, e.g. misalignment
- Indicates reasons for not vectorizing
  - Unsupported datatype → rewrite to use 32b indices vs. 64b
- Line numbers may not be what you expect
  - Inlining
  - Loop distribution, interchange, unrolling, collapsing

Source : References & Intel Xeon-Phi; http://www.intel.com/

Compiler-Based Autovectorization

- Compiler recreate vector instructions from the serial Program
- Compiler make decisions based on some assumption
- The programmer reassures the compiler on those assumptions
  - The compiler takes the directives and compares them with its analysis of the code
- Compiler checks for
  - Is "*p" loop invariant?
  - Are a, b, and c loop invariant?
  - Does a[] overlap with b[], c[], and/or sum?
  - Is "+" operator associative? (Does the order of "a
  - Vector computation on the target expected to be faster than scalar code?

```
#pragma simd reduction(+:sum)
     for(i=0;i<*p;i++) {
       a[i] = b[i]*c[i];
       sum = sum + a[i];
             }
```

- Compiler Confirms this loop :
  - "*p" is loop invariant
  - a[] is not aliased with b[], c[], and sum
  - sum is not aliased with b[] and c[]
  - "+" operation on sum is associative (Compiler can reorder the "add"s on sum)
  - Vector code to be generated even if it could be slower than scalar code

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon Phi : Coprocessors – Native Compilation
Complier Offload Pragmas

Compiler OPT report - contents

- Control over static reports
  - -opt-report [n=0-3] enables varying levels of detail
  - -opt-report-phase=[several options] enables specific detail
- Reveals info on various compiler optimization
  - Offloaded variables, –opt-report-phase=offload
  - Inlining, Vectorization
  - OpenMP parallelization, auto-parallelization
  - Loop permutations, loop distribution, loop distribution
  - Multiversioning of loops performed by compiler
    - Dynamic dependence checking, unit-stride for assumed shape arrays, trip-count checks, etc.
  - Prefetching
  - Blocking, unrolling, jamming
  - Whole-program optimization

Source : References & Intel Xeon-Phi; http://www.intel.com/

Summary: Tricks for Performance

- Use asynchronous data transfer and double buffering offloads to overlap the communication with the computation
- Optimizing memory use on Intel MIC architecture target relies on understanding access patterns
- Many old tricks still apply: peeling, collapsing, unrolling, vectorization can all benefit performance

Source : References & Intel Xeon-Phi; http://www.intel.com/

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An Overview of Multi-Core Processors

Conclusions

- An Overview of Intel Xeon-Phi Architectures, Programming on Xeon-Phi using Native Compilation and Compilation & Vectorization Techniques

Thank You

Any questions ?