C-DAC Four Days Technology Workshop

ON

Hybrid Computing – Coprocessors/Accelerators
Power-Aware Computing – Performance of Applications Kernels

hyPACK-2013
Mode 3 : Intel Xeon Phi Coprocessors

Lecture Topic :
Intel Xeon-Phi Coprocessor : Cilk Plus

***Venue** : CMSD, UoHYD ; **Date** : October 15-18, 2013*

An Overview of Xeon Phi – Prog. Shared Address Space Prog,. – Cilk Plus

Lecture Outline

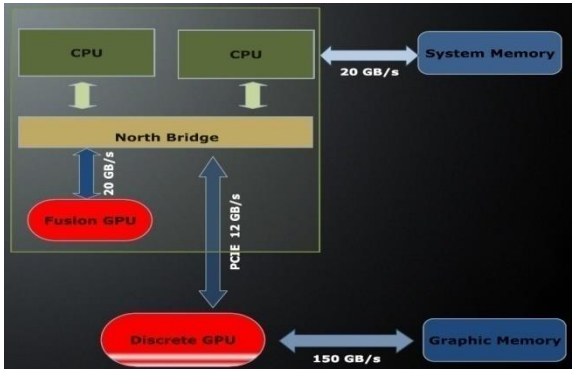
Following topics will be discussed

- Understanding of Xeon –Phi Architectures
- Programming on Xeon-Phi – Prog. -Cilk Plus
- Tuning & Performance – Software Threading

Intel Xeon-Phi
Shared Address Space Programming
Cilk Plus

Systems with Accelerators

A set (one or more) of very simple execution units that can perform few operations (with respect to standard CPU) with very high efficiency. When combined with full featured CPU (CISC or RISC) can accelerate the “nominal” speed of a system.



CPU — ACC

Single thread perf. **throughput**

CPU ACC.

Physical integration

CPU & ACC

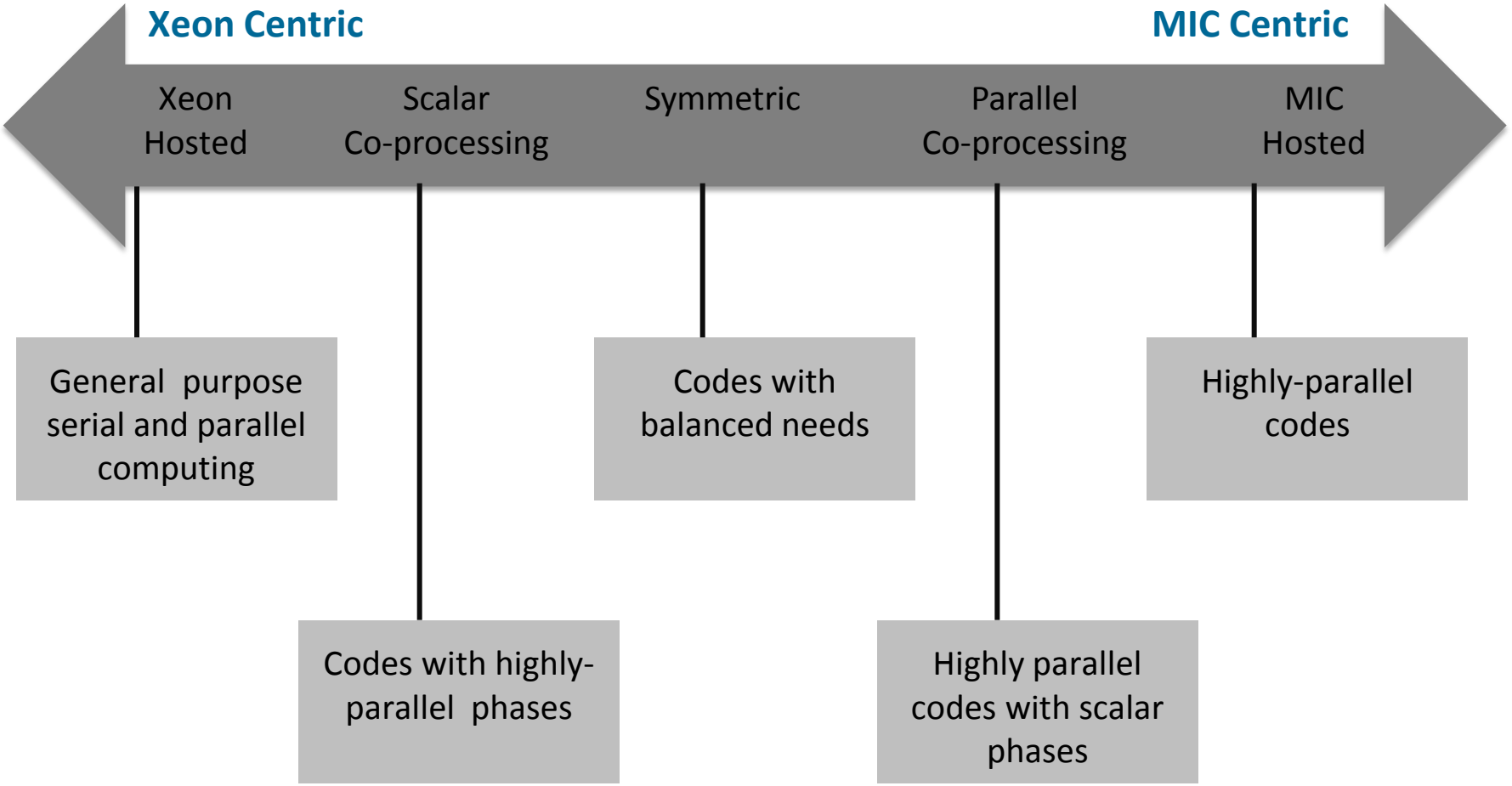
Architectural integration

CPU : Control Path & Data Path
ALU : Arithmetic and logic units
ACC: Accumulator
PC : Program counter
Micro-Instructions (Register transfer)

Source : NVIDIA, AMD, SGI, Intel, IBM Alter, Xilinux References

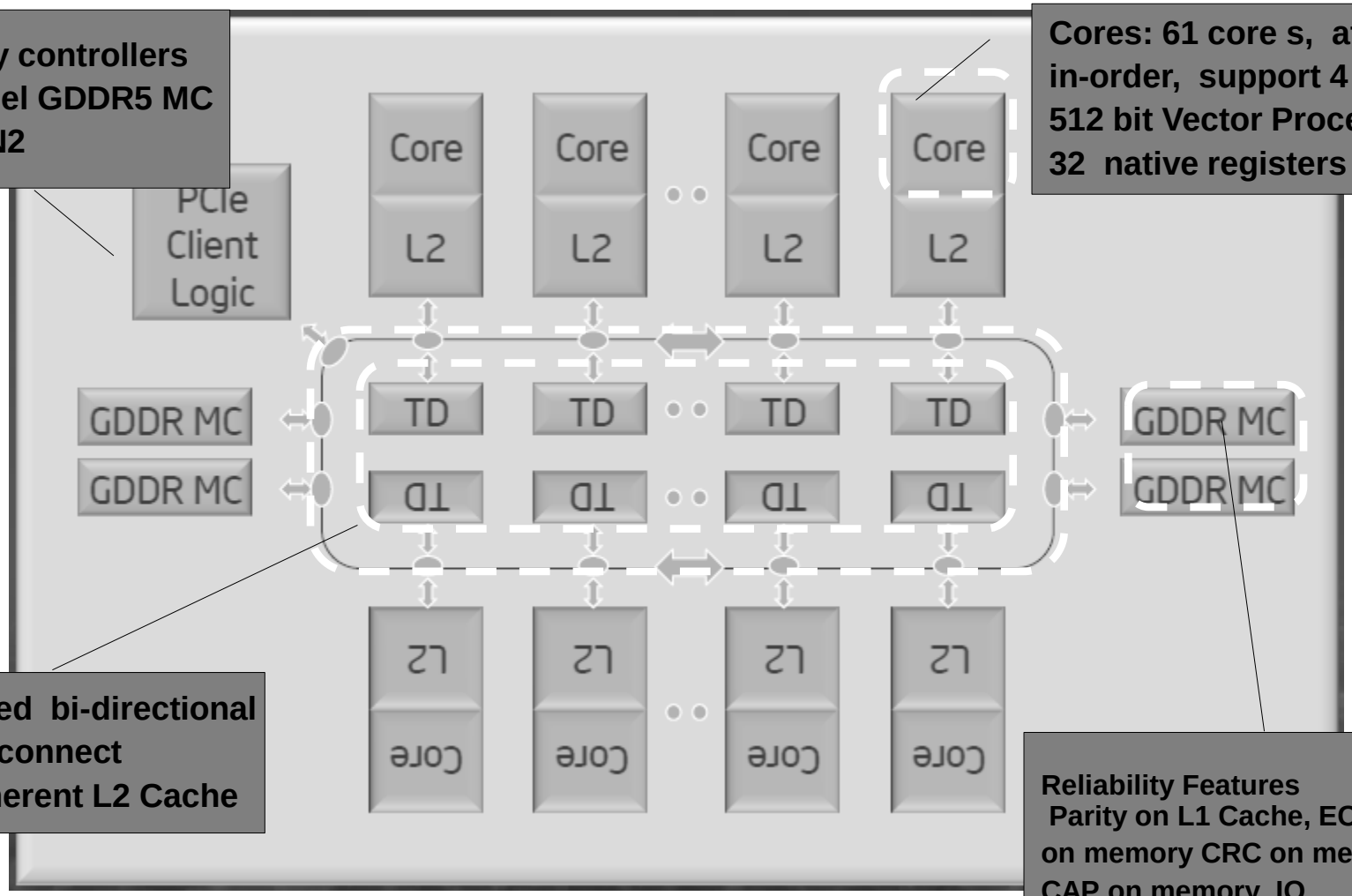
MIC Architecture, System Overview

Compute modes vision



Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel® Xeon Phi™ Architecture Overview



Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi
Shared Address Space Programming
Cilk Plus

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

- MIT Cilk – The original research project from MIT , culminating in Cilk-5.4.6. MIT Cilk was implemented as a source-to-source translator that converts Cilk code to C and them compiled the resulting C source.
  - Only supported C code with Cilk keywords
  - All parallel functions had to be marked with a cilk keyword
  - Cilk functions had to be spawned, not called

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

- Cilk++ - Compilers developed by Cilk Arts, Inc. Cilk Arts licensed the Cilk technology from MIT.
  - Only supported C++ code
  - Used a non-standard calling convention, meaning you had to use a cilk::context to
  - call Cilk functions from C or C++
  - Cilk files used the .cilk extension
  - Released by Intel as unsupported software through the WhatIf site

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

- Cilk++ - Intel Cilk Plus – Fully integrated into the Intel C/C++ compiler
  - Supports both C and C++
  - Uses standard calling conventions
  - Includes both task and data parallelism

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

- **Why to use it ?**
  - Intel® Cilk™ Plus is the easiest, quickest way to harness the power of both multicore and vector processing.
- **What is it ?**
  - Intel Cilk Plus is an extension to the C and C++ languages to support data
- **Primary Features :**

HPC

  - In efficient work-stealing scheduler provides nearly optimal scheduling of parallel tasks
  - Vector support unlocks the performance that's been hiding in your processors
  - Powerful hyperobjects allow for lock-free programming

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Primary Features :

- **Easy to Learn**
  - Only 3 new keywords to implement task parallelism
  - Serial semantics make understanding and debugging the parallel program easier
  - Array Notations provide a natural way to express data parallelism

- **Easy to Use**
  - Automatic load balancing provides good behaviour in multi-programmed environments
  - Existing algorithms easily adapted for parallelism with minimal modification
  - Supports both C and C++ programmers

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Primary Features :

Keywords : Simple, powerful expression of task parallelism:

- **cilk_for -** Parallelize for loops
- **cilk_spawn -** Specifies that a function can execute inparallel with the remainder of the calling function
- **cilk_sync -** Specifies that all spawned calls in a function must complete before execution continues

Other Options for Parallelism: Intel® Cilk™ Plus

C/C++ extension for fine-grained task parallelism. 3 keywords:

`_Cilk_spawn`

- Function call ***may*** be run in parallel with caller – up to the runtime

`_Cilk_sync`

- Caller waits for all children to complete

`_Cilk_for`

- Iterations are structured into a work queue
- Busy cores do not execute the loop
- Idle cores steal work items from the queue
- Countable loop Granularity is N/2, N/4, N/8, for trip count of N
- Intended use:
  - when iterations are not balanced, or
  - When overall load is not known at design time

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Primary Features :

Keywords : Simple, powerful expression of task parallelism:

- **Reducers:** Eliminate contention for shared variables among tasks by automatically creating views of them as needed and "reducing" them in a lock free manner.
- **Array Notation :** Data parallelism for arrays or sections of arrays.
- **Elemental Functions :** Define functions that can be vectorized when called from within an array notation expression or a **`#pragma simd`** loop
- **`#pragma simd:`** Specifies that a loop is to be vectorized

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi : Prog. Env. Cilk Plus

Cilk Plus Keywords

cilk_spawn and cilk_sync:

Example of Fibonacci number calculator program

❖ Sequential

```
int fib(int n)
{
  if (n < 2)
      return n;
      int x = fib(n-1);
      int y = fib(n-2);
      return x + y;
 }
```

❖ (With Cilk Plust Key Words)

```
int fib(int n)
{
  if (n < 2)
      return n;
      int x = cilk_spwan fib(n-1);
      int y = fib(n-2);
      cilk_sync;
      return x + y;
 }
```

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi : Programming Env.

Offload Code Examples

C/C+ Offload Pragma

```
#pragma offload target (mic)
#pragma omp parallel for reduction(+:pi)
 for (i = 0; i<count; i++) {
      float t = (float) (i+0.5/count);
      pi += 4.0/(1.0t*t);
 }
pi/ = count;
```

C/C++ Offload Pragma

```
#pragma offload target(mic)
      in(transa, transb, N, alpha, beta) \
      in(A:length(matrix_elements)) \
      in(B:length(matrix_elements)) \
      inout(C:length(matrix_elements))
         sgemm(&transa, &transb, &N, &N, &N,
& alpha, A, &N, B, & N, &beta, C &N);
```

Fortran Offload Directives

```
!dir$ omp offload target(mic)
!$omp parallel do
     do i = 1, 10
                A(i) = B(i) * C(i)
     enddo
```

C/C++ Language Extension

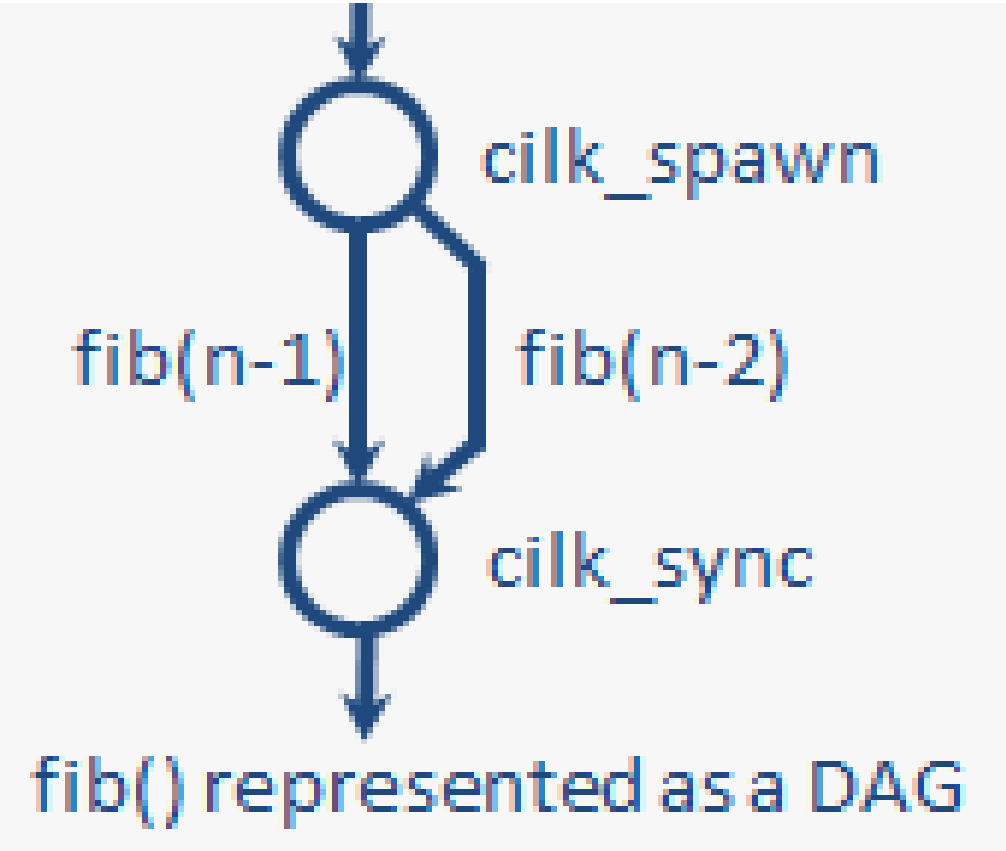
```
class_Cilk_Shared common {
    int data1;
    int *data2;
    class common *next;
    void process();
}
_Cilk_Shared class common obj1, obj2;
_Cilk_spawn _offload obj1.process();
_Cilk_spawn  _offload  obj2.process();
```

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi : Prog. Env. Cilk Plus

Cilk Plus Keywords

cilk_spawn and cilk_sync:



p://www.intel.com/

Intel Xeon-Phi : Prog. Env. Cilk Plus

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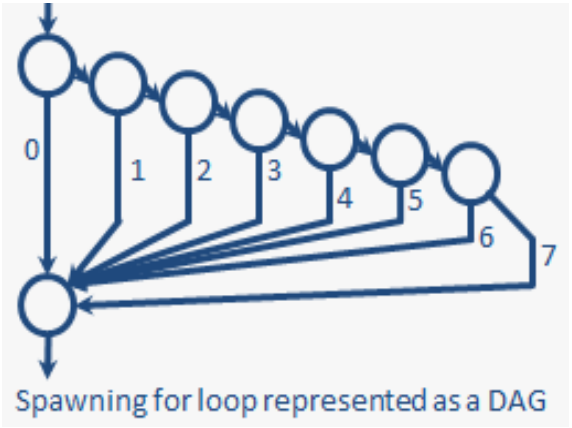
      cilk_sync;
      return x + y;
 }
```

Source : References & Intel Xeon-Phi; http://www.intel.com/

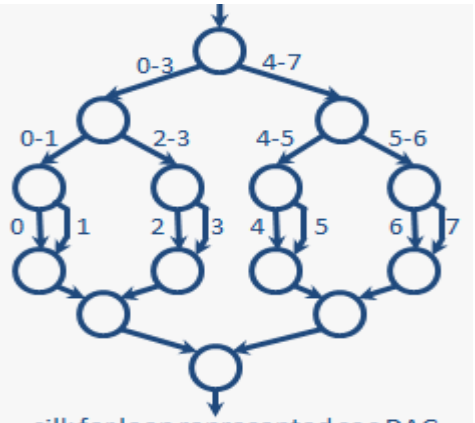
Intel Xeon-Phi : Prog. Env. Cilk Plus

Cilk Plus Keywords

Advantage of cilk_for over cilk_spawn



Spawning for loop represented as a DAG



cilk for loop represented as a DAG

cilk_spawn code

```
for (int i = 0; i < 8; ++i)
 {
   cilk_spawn do_work(i);
 }
cilk_sync;
```

cilk_for code

```
cilk_for (int i = 0; i < 8; ++i)
{    do_work(i);
}
```

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Cilk Plus Keywords

- **Features of cilk_spawn:**

  - **cilk_spawn** permits parallelism. It does not command it. cilk_spawn does not create a thread. It allows the runtime to steal the **continuation** to execute in another worker thread.
  - A **strand** is a sequence of instructions that starts or ends on a statement which will change the parallelism.
  - Permitting parallelism instead of commanding it is an aspect of the **serial semantics** of a deterministic **Intel Cilk Plus** application.
  - It is always possible to run an **Intel Cilk Plus** application with a single worker, and it should give identical results to the **serialization** of that program

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Cilk Plus Reducers : The Cilk Plus Reducer Library :

Lists

reducer_list_append: Creates a list by adding elements to the back.
reducer_list_prepend: Creates a list by adding elements to the front.

Min/Max

reducer_max: Calculates the maximum value of a set of values.
reducer_max_index: Calculates the maximum value and index of that value of a set of values.
reducer_min: Calculates the minimum value of a set of values.
reducer_min_index: Calculates the minimum value and index of that value of a set of values.

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Cilk Plus Reducers : The Cilk Plus Reducer Library :

Math Operators

reducer_opadd: Calculates the sum of a set of values.

Bitwise Operators

- reducer_opand: Calculates the binary AND of a set of values.
- reducer_opor: Calculate the binary OR of a set of values.
- reducer_opxor: Calculate the binary XOR of a set of values.

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Cilk Plus Reducers : The Cilk Plus Reducer Library :

```
void locked_list_test()
{  mutex m;
    std::list<char>letters;
  // Build the list in parallel
    cilk_for(char ch = 'a'; ch <= 'z'; ch++)
    {  simulated_work();
        m.lock();
        letters.push_back(ch);
        m.unlock();   }
 // Show the resulting list
    std::cout << "Letters from locked list: ";
    for(std::list<char>::iterator i = letters.begin(); i != letters.end(); i++)
    { std::cout << " " << *i;
    }std::cout << std::endl;}
```

Letters from locked list: y g n d t a w x e z q j o h b u f v c k i r p l m s

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Cilk Plus Reducers : The Cilk Plus Reducer Library :

```
void reducer_list_test()
{  cilk::reducer_list_append<char> letters_reducer;
  // Build the list in parallel
    cilk_for(char ch = 'a'; ch <= 'z'; ch++)
    {  simulated_work();
       letters_reducer.push_back(ch);
    }
// Fetch the result of the reducer as a standard STL list
    const std::list<char> &letters = letters_reducer.get_value();
  // Show the resulting list
    std::cout << "Letters from reducer_list:";
    for(std::list<char>::const_iterator i = letters.begin(); i != letters.end(); i++)
    { std::cout << " " << *i;
    }std::cout << std::endl;}
```

Letters from reducer_list: a b c d e f g h i j k l m n o p q r s t u v w x y z

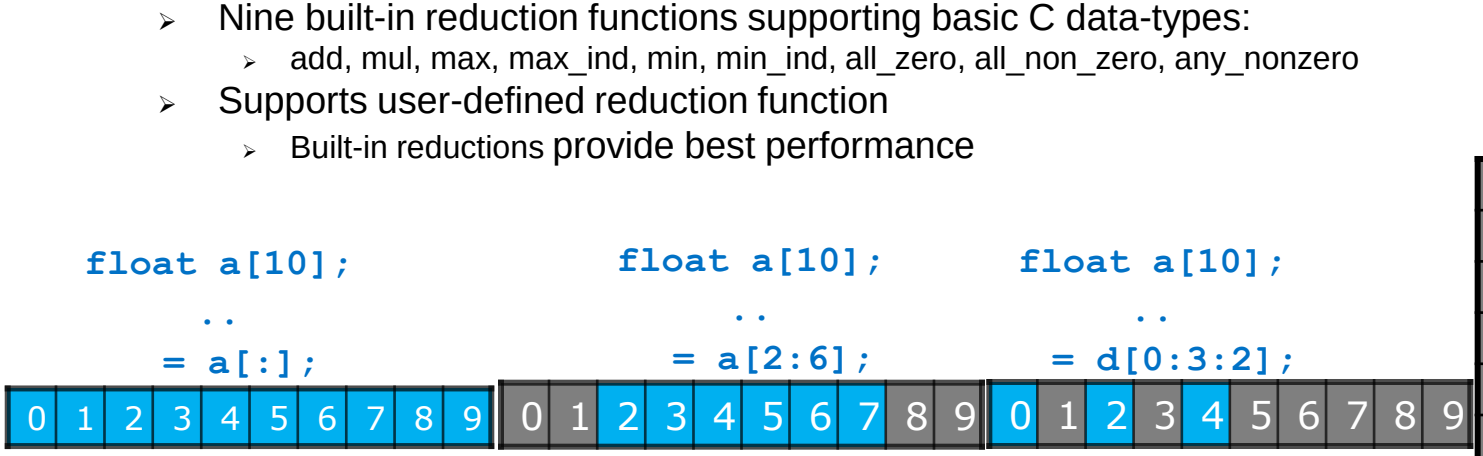
Source : References & Intel Xeon-Phi; http://www.intel.com/

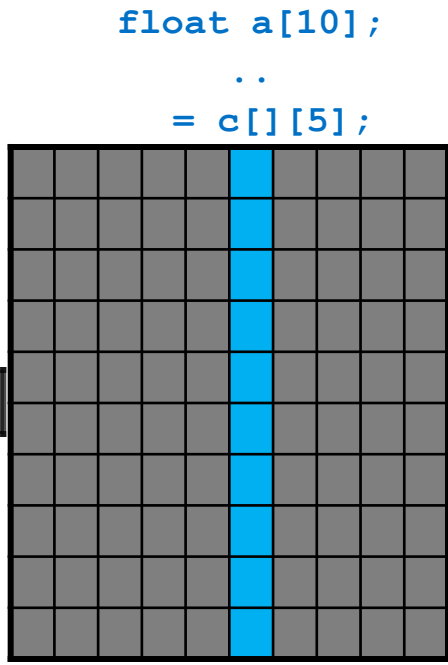
Intel® Cilk™ Plus Array Notation

- C/C++ Language extension supported by the Intel® Compiler
- Based on the concept of array-section notation:

```
<array>[<low_bound> : <len> : <stride>] [<low_bound> : <len> :
  <stride>]…
```

- C/C++ Operators / Function Calls
  - `d[:] = a[:] + (b[:] * c[:])`
  - `b[:] = exp(a[:]); // Call exp() on each element of a[]`
- Reductions combine array section elements to generate a scalar result
  - Nine built-in reduction functions supporting basic C data-types:
    - add, mul, max, max_ind, min, min_ind, all_zero, all_non_zero, any_nonzero
  - Supports user-defined reduction function
    - Built-in reductions provide best performance





Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Cilk Plus Array Notation

- Intel Cilk Plus includes extensions to C and C++ that allows for parallel operations on arrays.
- The intent is to allow users to express high-level vector parallel array operations. –
- This helps the compiler to effectively vectorize the code.
- Array notation can be used for both static and dynamic arrays.
- The extension has parallel semantics that are well suited for per-element operations that have no implied ordering and are intended to execute in data-parallel instructions.

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Cilk Plus Array Notation

A new operator [:] delineates an array section:

```
array-expression[lower-bound : length : stride]
```

- Length is used instead of upper bound as C and C++ arrays are declared with a given length.
- The three elements of the array notation can be any integer expression. The user is responsible for keeping the section within the bounds of the array.
- Each `argument to [:]` may be omitted if the default value is sufficient.
  - The default lower-bound is `0.`
  - The default length is the length of the array. If the length of the array is not known, length must be specified.
  - The default stride is 1. If the stride is defaulted, the second ":" may be omitted.

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

User-mandated Vectorization(pragma simd)

- SIMD (Single Instruction, Multiple Data) vectorization uses the **`#pragma simd`** pragma to enforce loop vectorization.
- Consider an example in C++ where the function **`add_floats()`** uses too many unknown pointers, preventing automatic vectorization. You can give a data-dependence assertion using the **`auto-vectorization`** hint via **`#pragma ivdep`** and let the compiler decide whether the **`auto-vectorization`** optimization should be applied to the loop. Or you can now enforce vectorization of this loop by using **`#pragma simd`**.

```
void add_floats(float *a, float *b, float *c,
                float *d, float *e, int n)
{  int i;
   #pragma simd
   for (i=0; i<n; i++){
     a[i] = a[i]+ b[i]+c[i]+d[i] + e[i];}
}
```

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Cilk Plus : User-mandated Vectorization(pragma simd)

- The one big difference between using the SIMD pragma and **`auto-vectorization`** hints is that with the SIMD pragma, the compiler generates a warning when it is unable to vectorize the loop. With **`auto-vectorization`** hints, actual vectorization is still under the discretion of the compiler, even when you use the **`#pragma vector`** always hint.

- If a **`#pragma simd`** annotated loop is not vectorized by the compiler, the loop holds its serial semantics.

- By default "**`#pragma simd`**" is set to "**`noassert`**".and compiler will issue a warning if the loop fails to **`vectorize`**.

- To direct the compiler to assert an error when the **`#pragma simd`** annotated loop fails to vectorize , add the "assert" clause to the **`#pragma simd`**

Intel® Cilk™ Plus Technology: Elemental Function

- Allow you to define data operations using scalar syntax
- Compiler apply the operation to data arrays in parallel, utilizing both SIMD parallelism and core parallelism

Programmer	Build with Intel Cilk Plus Compiler
1. Writes a standard C/C++ scalar syntax 2. Annotate it with **__declspec**(vector) 3. Use one of the parallel syntax choices to invoke the function	1. Generates vector code with SIMD Instr. 2. Invokes the function iteratively, until all elements are processed 3. Execute on a single core, or use the task scheduler, execute on multicores

```
__declspec (vector)
double BlackScholesCall(double S,
                        double K,
                        double T)
                  {
 double d1, d2, sqrtT = sqrt(T);
d1 = (log(S/K)+R*T)/(V*sqrtT)+0.5*V*sqrtT;
          d2 = d1-(V*sqrtT);
return S*CND(d1) - K*exp(-R*T)*CND(d2);
                  }
```

```
Cilk_for (int i=0; i < NUM_OPTIONS; i++)
     call[i] = BlackScholesCall(SList[i],
                                KList[i],
                                TList[i]);
```

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Elemental Functions

- An elemental function is a regular function, which can be invoked either on scalar arguments or on array elements in parallel. You define an elemental function by adding

  "__declspec(vector)" (on Windows*) and

  "__attribute__((vector))" (on Linux*) before

- the function signature:

```
__declspec (vector)
double  ef_add (double x, double y)  {return x + y;}
```

When you declare a function as elemental the compiler generates a short vector form of the function, which can perform your function's operation on multiple arguments in a single invocation.

Source : References & Intel Xeon-Phi; http://www.intel.com/

Intel Xeon-Phi - for Parallelism: Intel® Cilk™ Plus

Elemental Functions

The vector form of the function can be invoked in parallel contexts in the following ways:

1. From a for-loop. It gets auto-vectorized; a loop that only has a call to an elemental function is always vectorizable, but the **`auto-vectorizer`** is allowed to apply performance heuristics and decide not to vectorize the function.
2. From a for-loop with **`pragma simd`**. If the elemental function is called from a loop with "**`pragma simd`**", the compiler no longer does any performance heuristics, and is guaranteed to call the vector version of the function.
3. From a **`cilk_for`**
4. From an array notation syntax. .

Summary: Tricks for Performance

- Use asynchronous data transfer and double buffering offloads to overlap the communication with the computation
- Optimizing memory use on Intel MIC architecture target relies on understanding access patterns
- Many old tricks still apply: peeling, collapsing, unrolling, vectorization can all benefit performance

Source : References & Intel Xeon-Phi; http://www.intel.com/

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An Overview of Multi-Core Processors

Conclusions

- An Overview of Xeon-Phi Architectures, Programming on based on Shared Address Space Platforms – Cilk Plus, Performance of Software threading are discussed.

Thank You

Any questions ?