C-DAC Four Days Technology Workshop

ON

Hybrid Computing – Coprocessors/Accelerators
Power-Aware Computing – Performance of Applications Kernels

hyPACK-2013
(Mode-1:Multi-Core)

Lecture Topic:

Multi-Core Processors : Multi-Core Architecture Part-I

Venue : CMSD, UoHYD ; Date : October 15-18, 2013

An Overview of threading

Lecture Outline

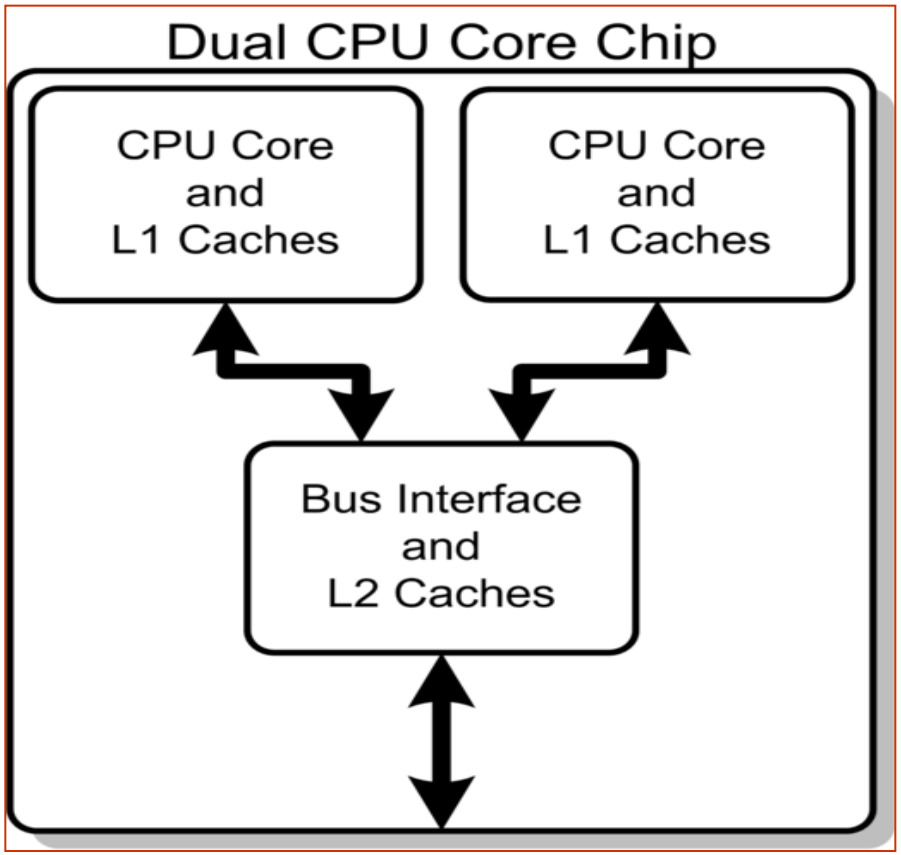
Following Topics will be discussed

- Introduction
- Understanding of Intel Multi-Core Architectures
- Multithreading, Superthreading & HyperThreading
- Case Studies & Examples

Dual-Core Processor

Conceptual diagram of

- A dual-core CPU, with
- CPU-local Level 1 caches, and
- Shared, on-chip Level 2 caches

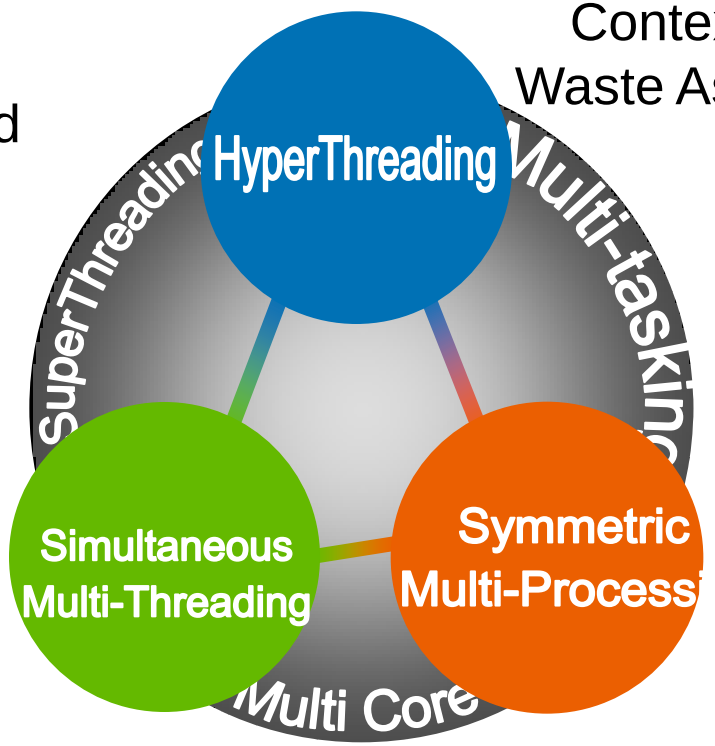


An Overview of threading

SMP and Cluster Platforms based on

Industry Standard Servers

Single Threaded CPU
Preemptive vs. co-operative Multitasking
Context, process and Thread
Waste Associated with Threads
Time Slicing
I/O Threads



Implementing Hyper-threading
- Caching & SMT

Implementing Hyper-threading
- Replicated
- Partitioned
- Shared

Source : http://www.intel.com ; htpp://www.amd.com; Reference : [6], 29], [31]

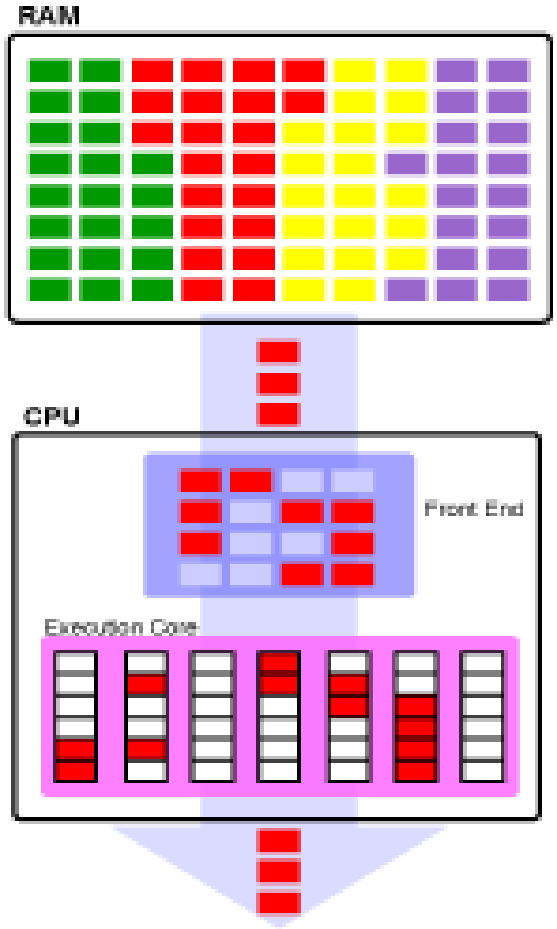
Multi-threading

- Understand more about multi-threading
- Understand more about multi-processing system
- Understand Hyper-threading
- The concept of **Simultaneous Multi-Threading** (**SMT**) – known as "**Hyper-threading**")
  - Multi-Tasking – Earlier Generation CPU's handle **Multi-tasking**
  - **SMT** – allows CPU to run more than one program at the same time

Conventional Multi-threading

❖ Out of Order Execution

- Not execute sequentially
- Reschedule the instructions
- Arrange them back after execution
- Looks as if an ordered sequential stream of instruction is executing
- Only CPU knows about execution order
- Still execution block is not fully utilized



❖ Time Slicing

❖ Empty Pipe-line stages; CPU can issue upto to four instructions per clock cycle.

Source : http://www.intel.com

Reference : [6], [29], [31]

Co-operative Multitasking

❖ Co-operative Multi-tasking

- Running programs to co-operate with each other and with OS in order to share the CPU among themselves in a fair and equitable manner.
  - Multiple program are loaded into memory
  - Both h/w and OS are involved
  - OS rapidly switch between running programs within a time frame(time slice).
  - Some time job with long execution time suffer from starvation
  - Still some execution block is utilized
- Designated Time Slice for execution of Program
- Problems : Some programs - Monopolize the CPU – System Grid to halt

Pre-emptive Multitasking

❖ Pre-emptive Multi-tasking

- Strictly enforced rules and kicks each program of the CPU once its time slice is up.
  - Memory Protection – OS makes sure that each program makes use the memory space allocated to it and it alone.
  - Instructions are fetched, decoded, and re-ordered & executed.
- Program is walled-off/Only one program on the system

Co-operative Multi-tasking & Pre-emptive Multi-tasking

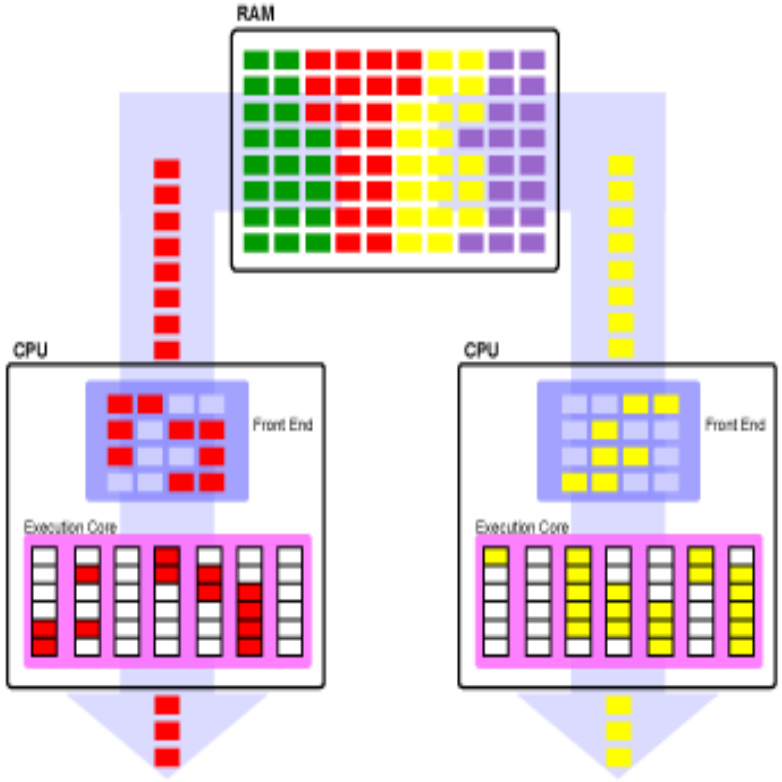
- Context Switches : currently executing process's context, flushing the CPU, and loading he next process's context
- A context Switch for a full-fledged multi-threaded process will obviously take a lot longer than a context switch for an individual thread within a process.
- Hardware support
- Wasting a number of CPU cycles
- Concept of Thread switches

An Overview of threading

- Issues & Challenges
  - Process, context and thread
  - Multi-tasking: Each program has a mind of its own
    - Pipeline bubbles
    - Number of Instructions per clock cycle
  - Time slicing – up-restore- context switches
  - The concept of “State” – Halting /Restoring
  - Wasting number of number of CPU cycles…
  - Execution efficiency improves ?

Symmetric Multiprocessors (SMPs) : Issues

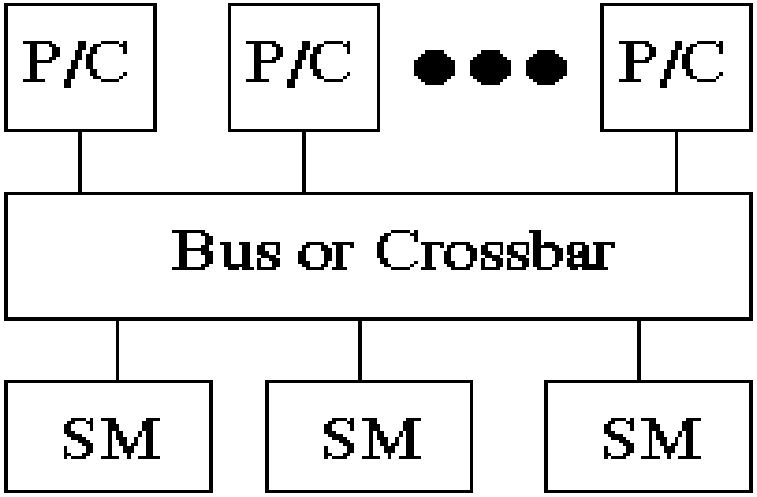
- Two processors is involved.
- OS schedule two processes for execution by either CPU
- Not allowed to monopolize
- Less waiting time
- Number of empty execution slots doubled
- Efficiency - No improvement in CPU utilization
- Time Slicing Issues



Reference : [6], [29], [31]

Symmetric Multiprocessors (SMPs) : Issues

(Contd…)



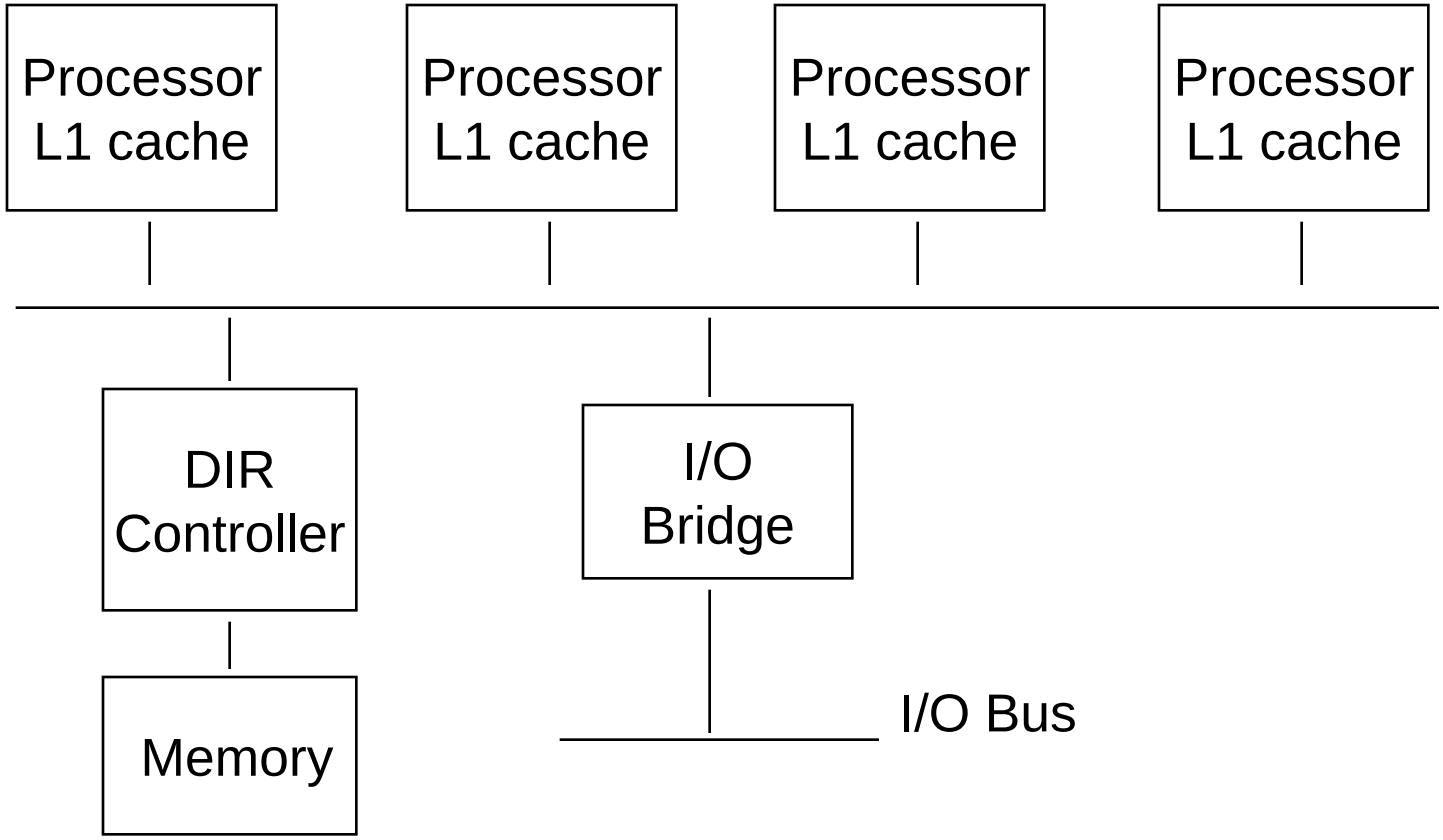
P/C : Microprocessor and cache; SM : Shared memory

- Uses commodity microprocessors with on-chip and off-chip caches.
- Processors are connected to a shared memory through a high-speed snoopy bus

Symmetric Multiprocessors (SMPs) : Issues

(Contd…)

All processors see same image of all system resources



Symmetric Multiprocessors (SMPs) : Issues (Contd…)

- On Some SMPs, a crossbar switch is used in addition to the bus.
- Scalable upto:
  - 4-8 processors (non-back planed based)
  - few tens of processors (back plane based)
- Equal priority for all processors (except for master or boot CPU)
- Memory coherency maintained by HW
- Multiple I/O Buses for greater Input Output

Symmetric Multiprocessors (SMPs) : Issues

(Contd…)

- Bus based architecture :
  - Inadequate beyond 8-16 processors
- Crossbar based architecture
  - multistage approach considering I/Os required in hardware
- Clock distribution and HF design issues for backplanes

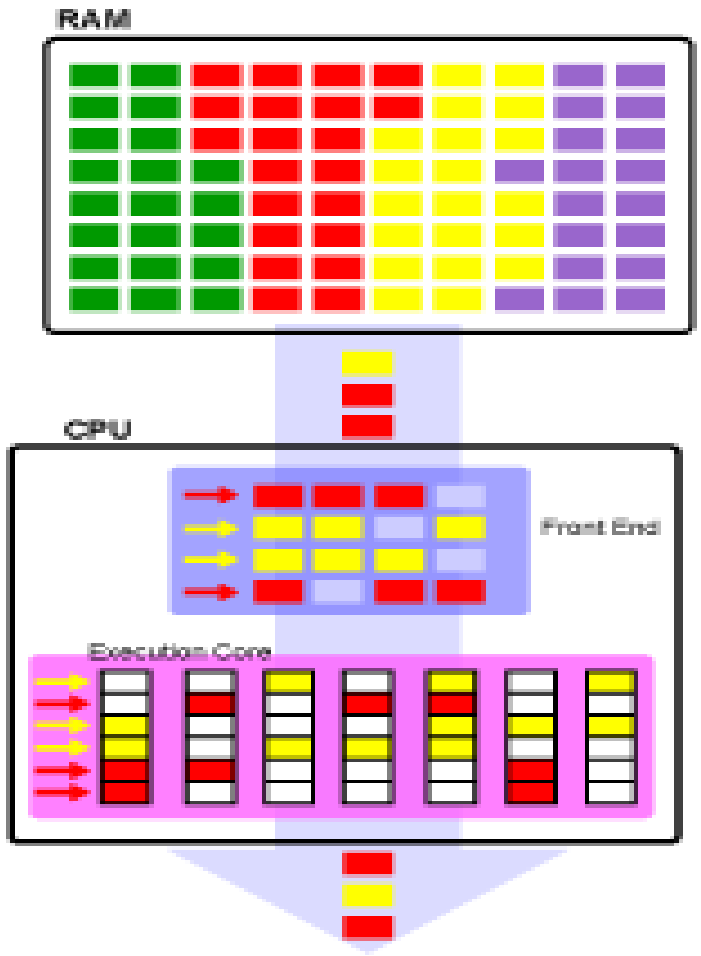
Commercial Symmetric Multiprocessors (SMPs) : IBM R690

- Limitation is mainly caused by using a centralized shared memory and a bus or cross bar interconnect which are both difficult to scale once built.

Superthreading with Multi threaded processor

Time-slice multi threading

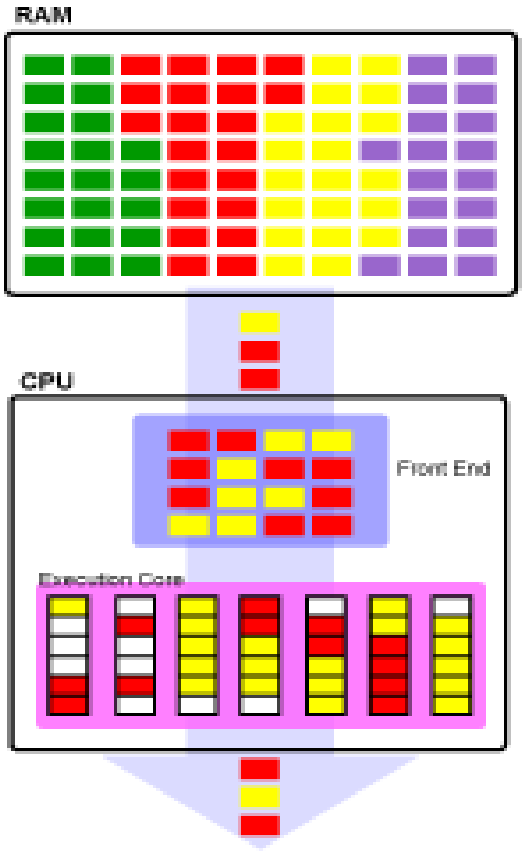
- Processor that use this technique is called multi threaded processor.
- Capable of executing more than one thread at a time.
- Front end (instruction queue) issue four instruction simultaneously
- All four instruction comes from single thread only.
- Deals with memory access latency but don't deals with poor instruction level parallelism



Reference : [6], [29], [31]

Introduction Hyperthreading

- Takes superthreading to next lev
- Hyper threading is simple super out restriction that all instruction from same thread only
- Its strength is it allows the sched maximum flexibility to fill executi
- Make efficient use of available e resources by keeping the execut busier

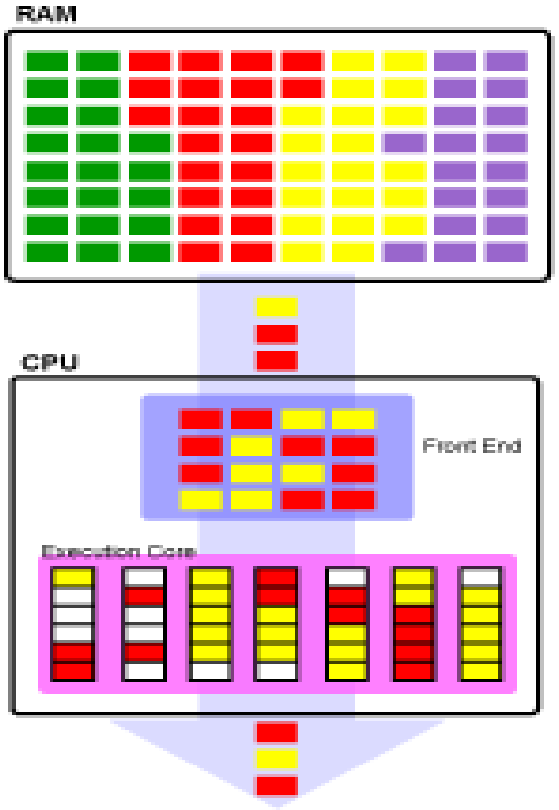


- The implementation of HT technology was the first SMT solution for general processors from Intel.

Source : http://www.intel.com ; Reference : [6], 29], [31]

Hyper threading :The next step introduction

- Hyper threading is simple super threading with out restriction that all instruction should come from same thread only
- Its strength is it allows the scheduling logic maximum flexibility to fill execution slots.
- Make efficient use of available execution resources by keeping the execution core busier



- Inside a processor with HT technology, two threads share resources from a single core - Threads are referred to as logical processors.

Source : http://www.intel.com ; Reference : [6], 29], [31]

Implementing Hyperthreading

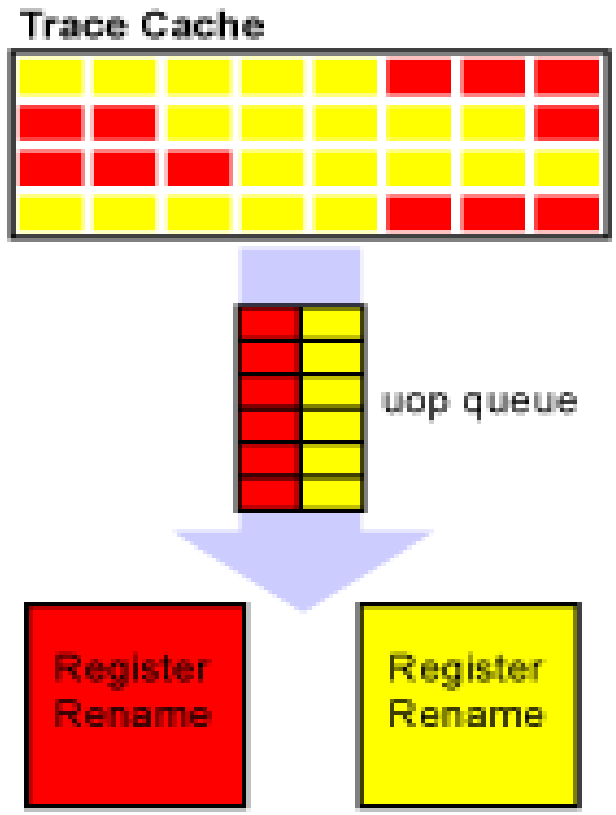
Hyper threading is implemented by dividing processor micro architectural resources into three types.

- Replicated :
  - Instruction Pointer
  - various other architectural register
- partitioned :
  - Re-order buffers
  - Load/Store buffers
- shared :
  - Caches : trace cache, L1, L2, L3
  - Micro Architectural Registers
  - Execution units

Source : http://www.intel.com
Reference : [6], 29], [31]

Hyper-threading : Partitioned Resources

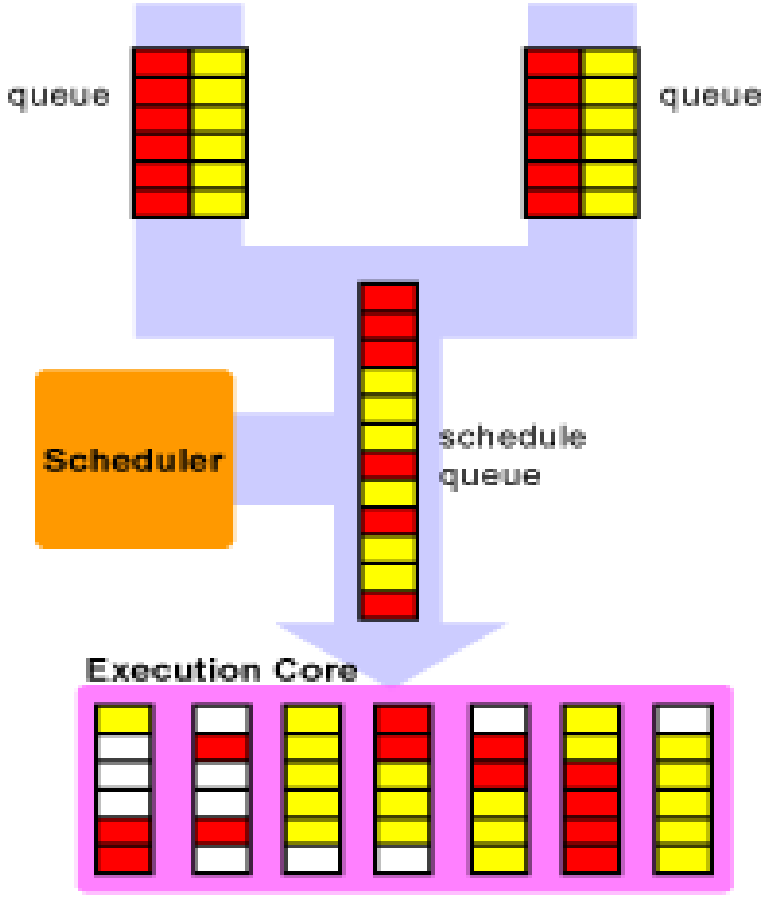
- The most partitioned resources are mostly to be found in the form of queues that decouple the major stages of the pipeline from one another.
- There are two kind of partitioned resources
  - 1) Statically partitioned
  - 2) Dynamically partitioned



Source : http://www.intel.com ; Reference : [6], 29], [31]

Hyper-threading : Partitioned Resources

- Xeon's scheduling queues are dynamically partitioned in order to keep one logical processor from monopolizing them
- There is limitation on number of entries that each logical processor can use



Source : http://www.intel.com ; Reference : [6], 29], [31]

Hyper-threading : Partitioned Resources

- Shared resources are at the heart of Hyper-threading
- More resources that can be shared between logical processors ,the more efficient hyper-threading can be squeezing the maximum amount of computing power achieved
- Some shared resources are integer unit,floating point unit,register file etc.

Source : http://www.intel.com ; Reference : [6], 29], [31]

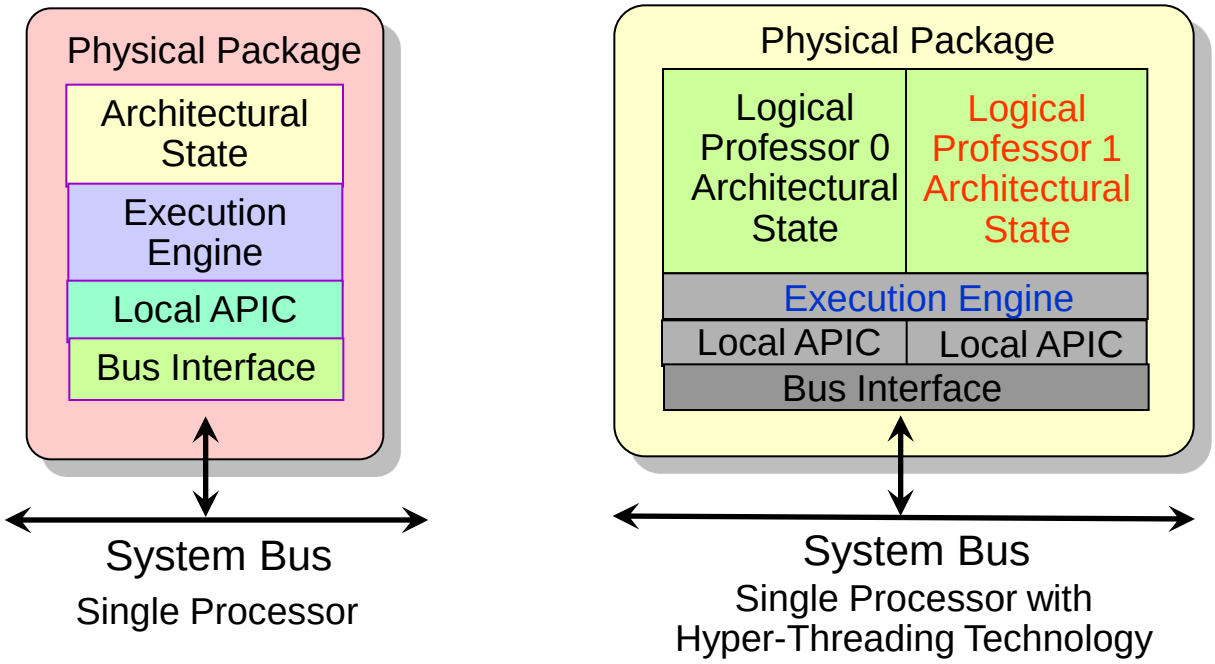
Hyper-threading : Partitioned Resources

- Cache coherency problems associated with SMP all but disappear.
- Both logical processor on an SMT system share same resources.
- However, since both logical processors share the same cache the prospect of cache conflicts increase.

Source : http://www.intel.com ; Reference : [6], 29], [31]

Hyper-threading : Partitioned Resources

- Hyper-threading (HT) technology is a hardware mechanism where multiple independent hardware threads get to execute in a single cycle on a single super-scalar processor core.

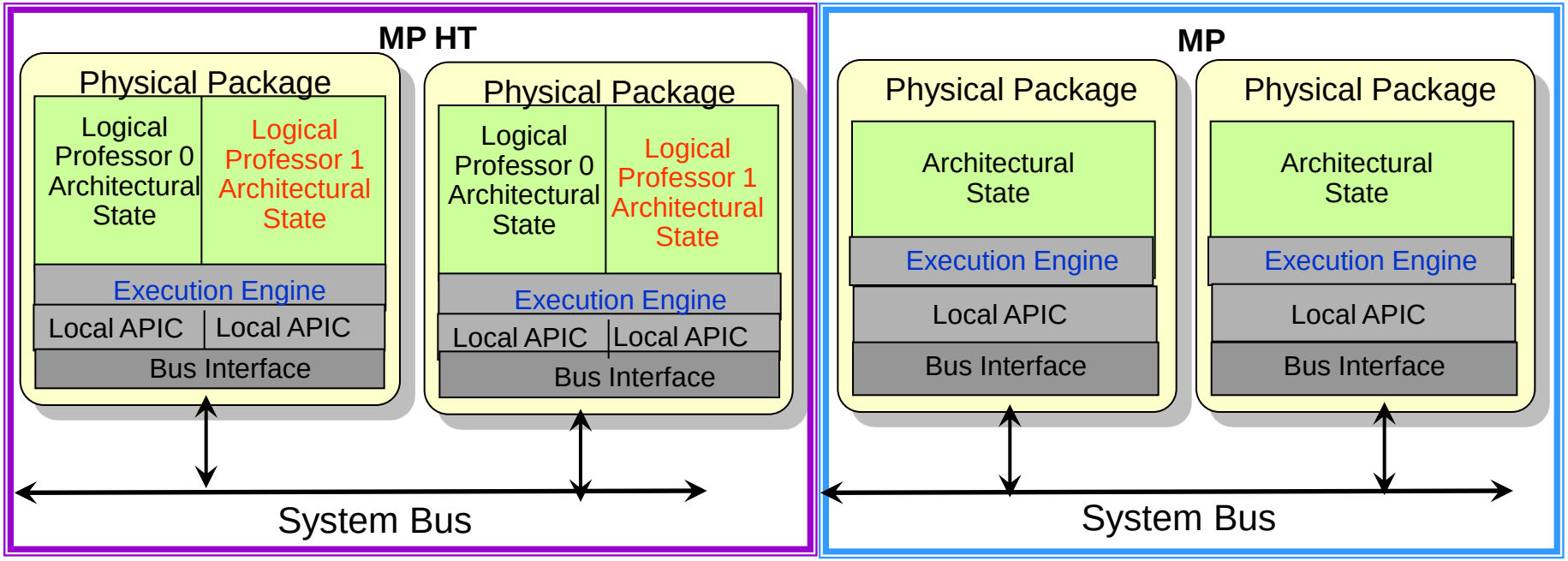


Single Processor System without Hyper-Threading Technology and Single Processor System with Hyper-Threading Technology

Source : http://www.intel.com ; Reference : [6], [10], [19], [23], [24],[29], [31]

Hyper-threading Technology

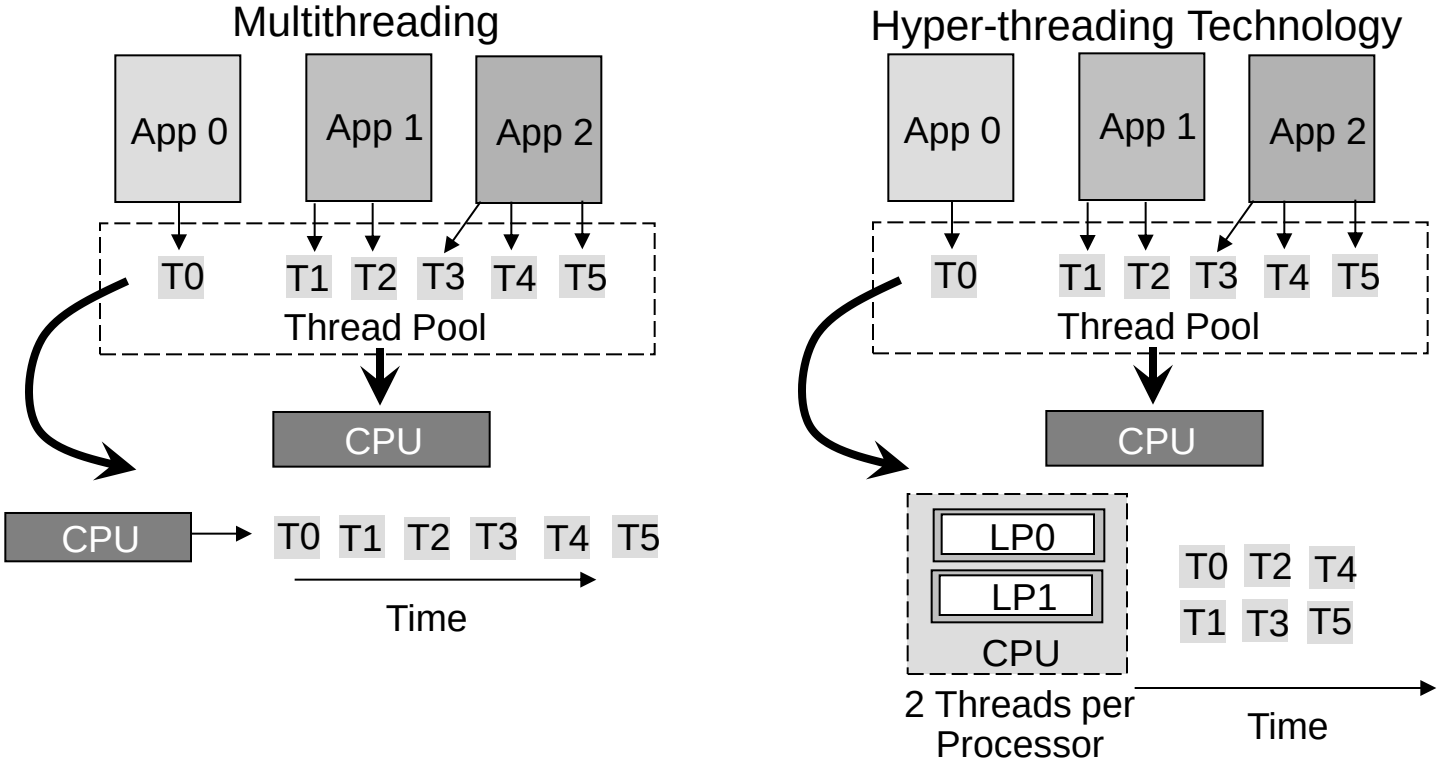
- Multi-processor with and without Hyper-threading (HT) technology



Source : http://www.intel.com ; Reference : [6], [29]. [31]

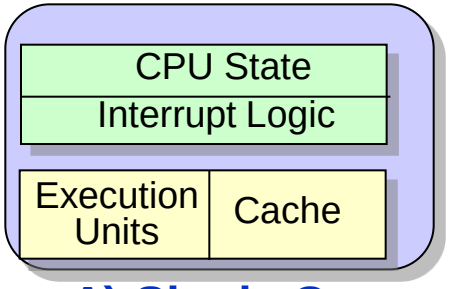
Multi-threaded Processing using Hyper-Threading Technology

- Time taken to process *n* threads on a single processor is significantly more than a single processor system with HT technology enabled.

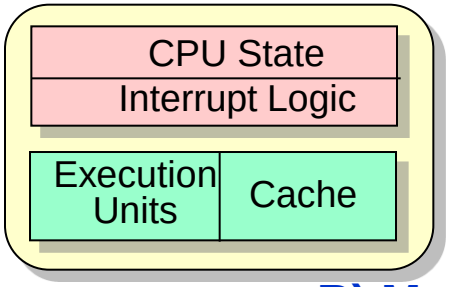


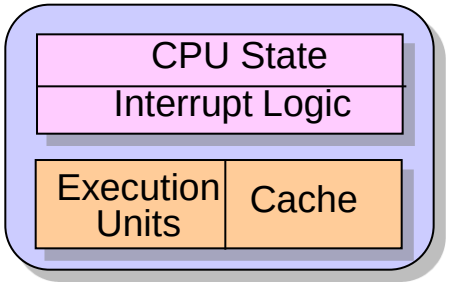
Source : http://www.intel.com ; Reference : [6], [29], [31]

Simple Comparison of Single-core, Multi-processor, and multi-Core Architectures

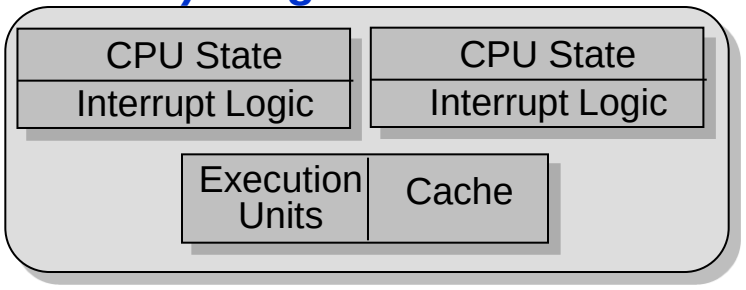


A) Single Core

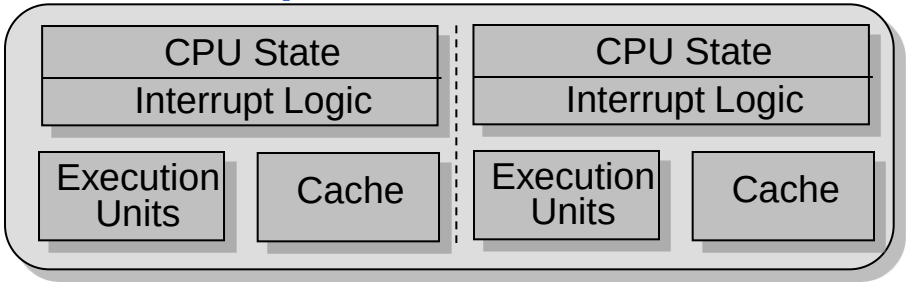




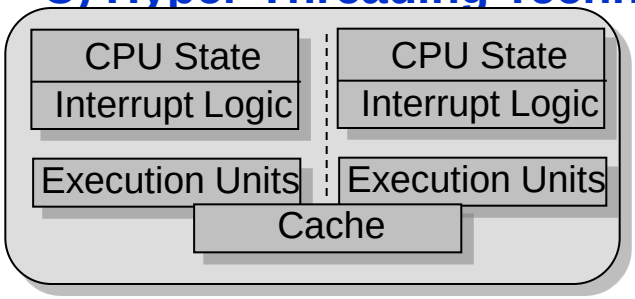
B) Multi Processor



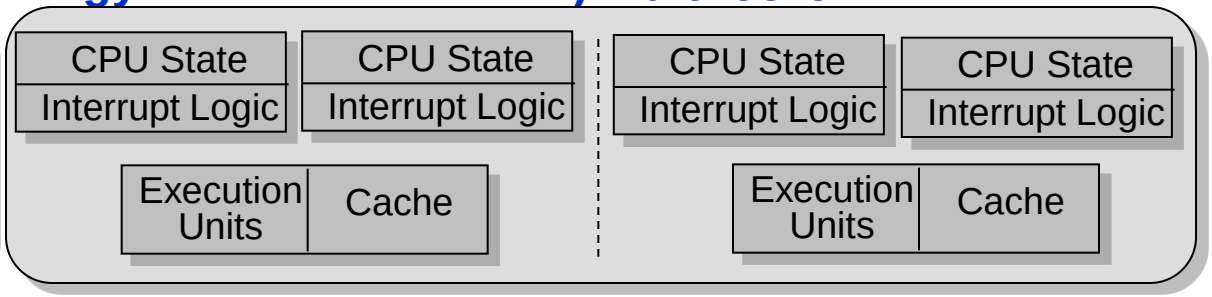
C) Hyper-Threading Technology



D) Multi-core



E) Multi-core with Shared Cache

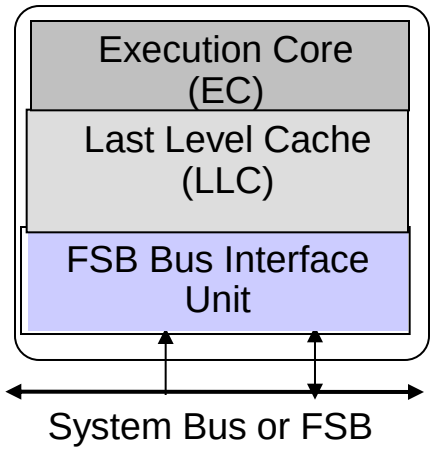


F) Multi-core with Hyper-threading Technology

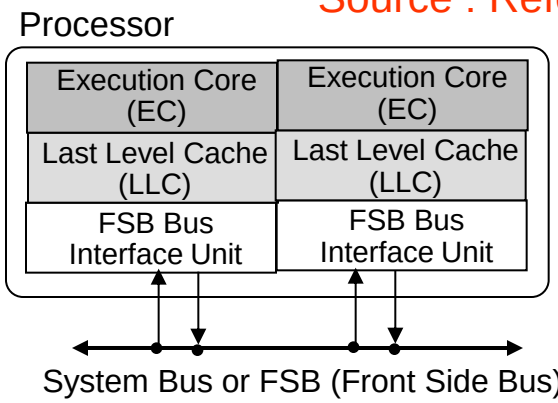
Source : http://www.intel.com ; Reference : [4],[6], [29], [31]

Multi-Core Processor Configurations

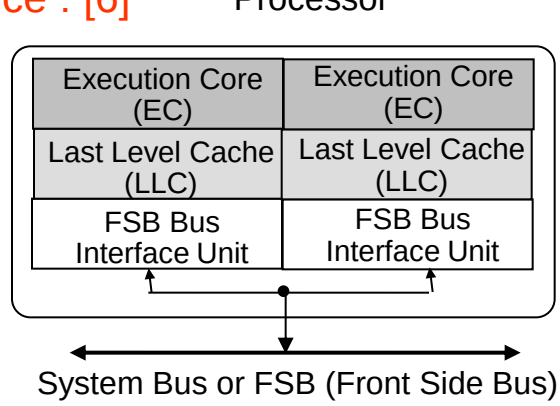
Source : Reference : [6]



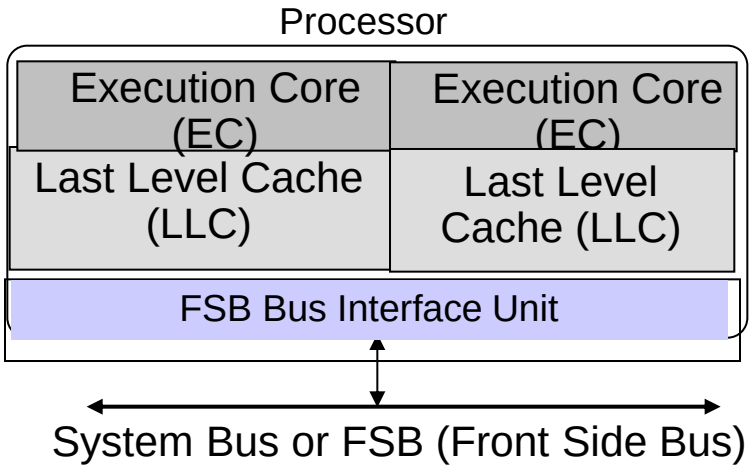
(a) Single Core Processor



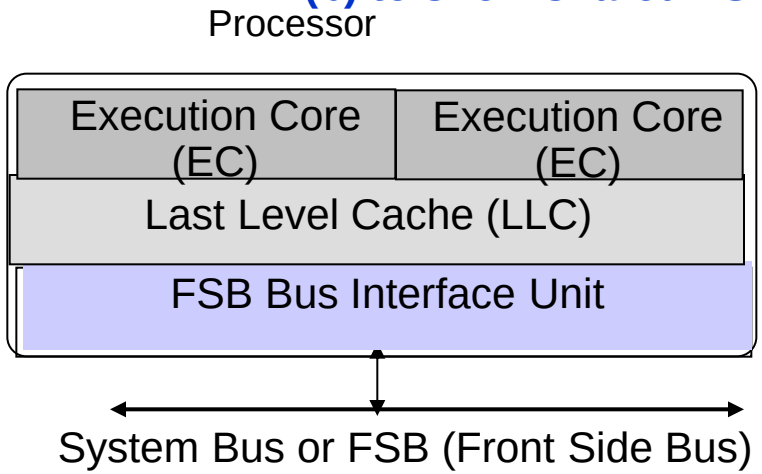
(b) Multi-Core Processor with Two Cores and Individual FSB



(c) Actual representation of (b) to show shared FSB



(d) Multi-Core Processor with Two Cores and Shared FSB



(e) Multi-Core Processor with Two Cores and Shared LLC and FSB

Multi Core : Programming Issues

- Out of Order Execution
- Preemptive and Co-operative Multitasking
- SMP to the rescue
- Super threading with Multi threaded Processor
- Hyper threading the next step (Implementation)
- Multitasking
- Caching and SMT

Conclusions

- An overview of Threading
- An overview of Superthreading & HyperThreading
- Multi Core Processor Configurations of various Systems
- An Overview of Multi-Core Architecture : Part I

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Thank You

- *Any questions ?*